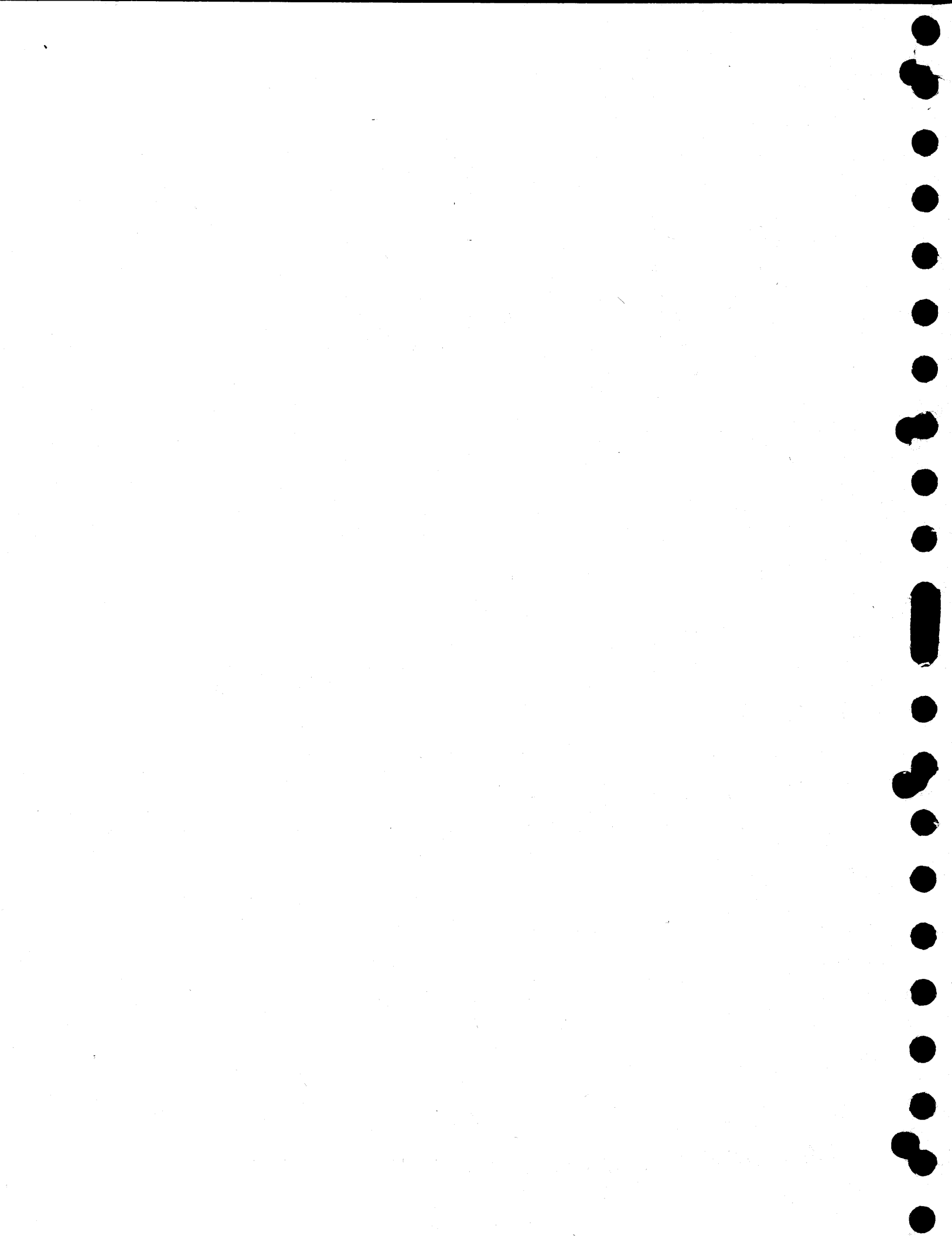


CONTROL DATA[®] **DISK STORAGE UNIT**

MAINTENANCE AIDS

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PREFACE

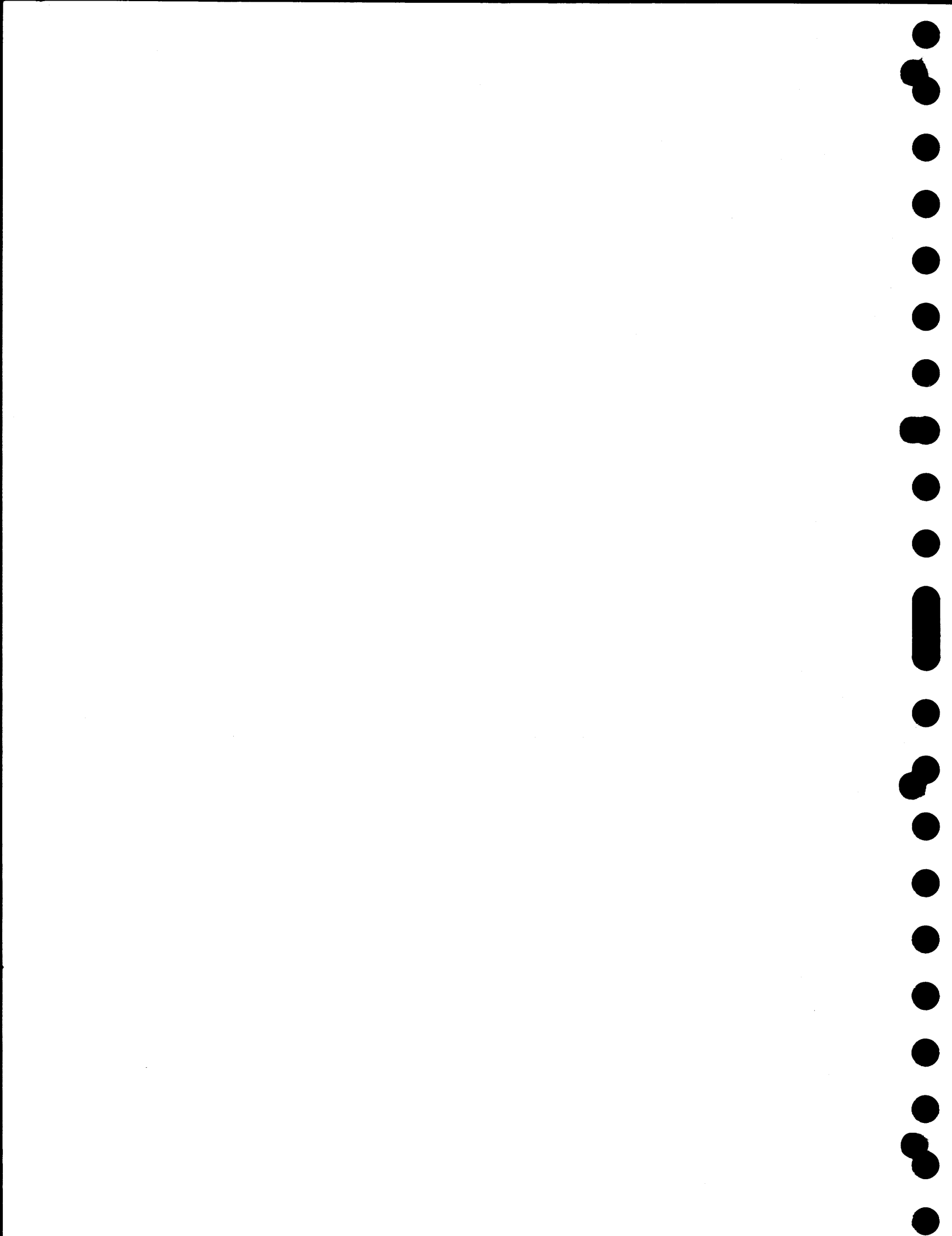
Customer engineering material for the CONTROL DATA® Disk Storage Unit is contained in four separate manuals, which provide all information needed to install, operate, and maintain the unit:

General Description, Operation,
Installation and Checkout, Theory of
Operation, Maintenance

Diagrams, Wire Lists

Illustrated Parts List

Maintenance Aids



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Information for these sections is included in Disk
Storage Unit. General Description, Operation,
Installation and Checkout, Theory of Operation,
Maintenance Manual.

SECTION 1
GENERAL DESCRIPTION

SECTION 2
OPERATION

SECTION 3
INSTALLATION AND CHECKOUT

SECTION 4
THEORY OF OPERATION



SECTION 5

DIAGRAMS

Information for this section is contained in Disk Storage Unit Diagrams, Wire Lists Manual.

SECTION 6

MAINTENANCE

Information for these sections is included in Disk Storage Unit General Description, Operation, Installation and Checkout, Theory of Operation, Maintenance Manual.



SECTION 7

MAINTENANCE AIDS



PART 1

DISCRETE COMPONENT
CIRCUIT DESCRIPTIONS



MAINTENANCE AIDS

GENERAL

Section 7 contains information on logic circuits, the criteria used in determining the further usability of read/write heads and disk packs, and the tester card used in the Maintenance section.

LOGIC

The logic used in this device consists of two styles of circuits: discrete component and integrated circuits. Discrete component circuits contain individually identifiable resistors, capacitors, transistors, etc.

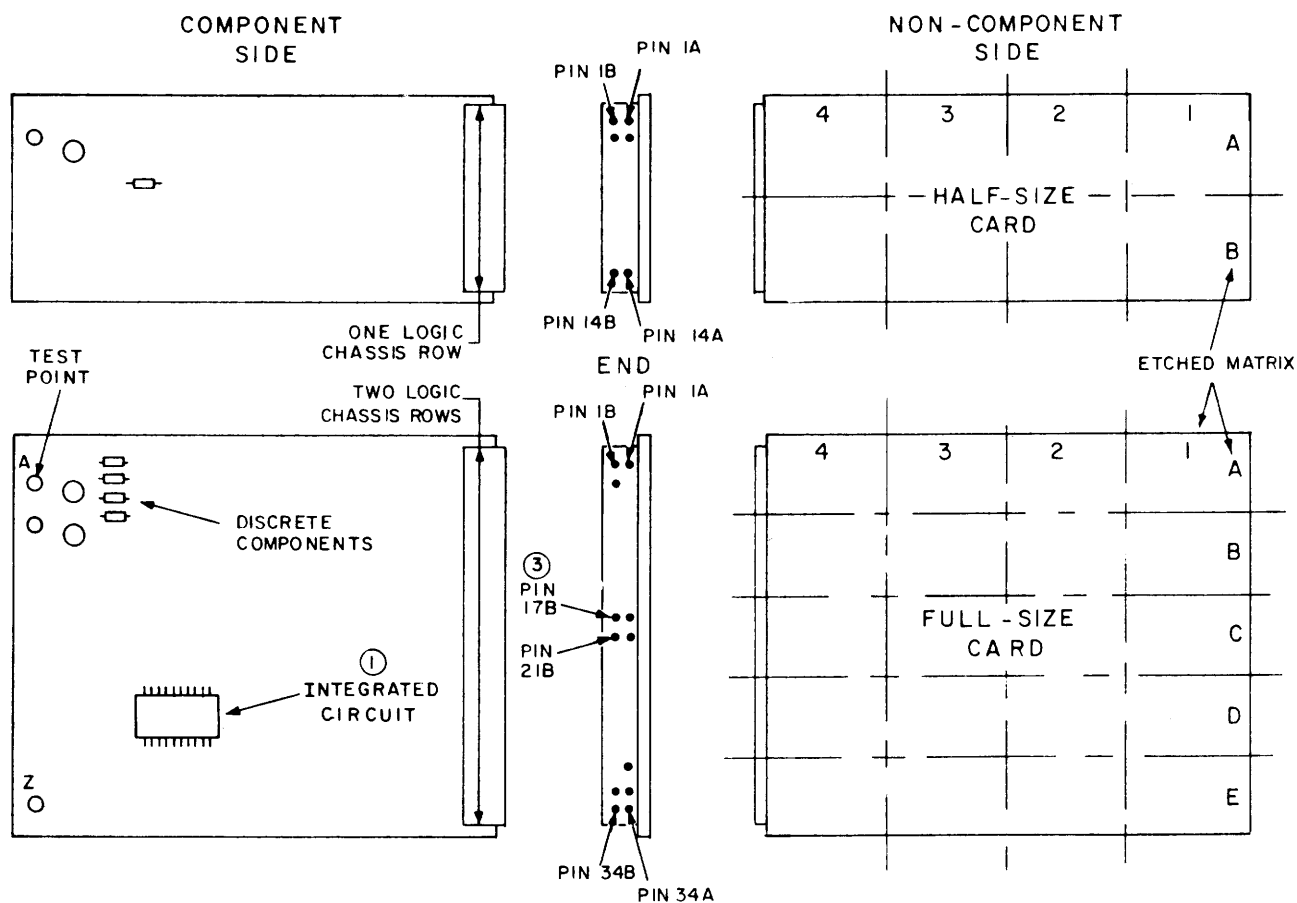
PHYSICAL DESCRIPTION

All components of the logic cards (Figure 7-1) are mounted on one side of a printed circuit board (PCB). Two sizes of PCB are used. The 6.075 x 2.3 inch PCB is the basis for the half-size card (plugs into one logic row). The 6.075 x 4.85 inch PCB is used on the full-size card. The latter card spans two rows of the logic chassis. The female connector of the cards mate with wire wrap pins extending through the chassis wire wrap board. The logic cards functions are dispersed from the reverse ends of these pins through wiring installed using the wire wrap technique. Cards installed in the logic chassis are restricted from vertical and horizontal movement by card guide spacers.

Numerical designators (1 through 99) are etched on the non-component side of the board identify each transistor. A 4-character alpha-numeric designator is etched on the non-component side of the board to identify the card type. A matrix code (alphanumeric) also appears on this side. Non-amplifying components such as integrated circuits, resistors, capacitors, diodes, etc., are not marked.

Pin Assignments

Half-size cards are equipped with a 28-pin (sockets) connector, while the full-size card contains a 62-pin connector. Connectors are mounted along the shorter dimension on the component side of the board.



NOTES:

- ① INTEGRATED CIRCUIT LOCATED AT BOARD MATRIX D2
2. ON LOGIC DRAWINGS, CARD PINS AND MATRIX LOCATIONS, ARE PRECEDED BY 3 DIGITS THAT IDENTIFY LOCATION OF CARD IN LOGIC CHASSIS (A23, POSITION 23 IN CHASSIS ROW A)
- ③ PINS 18, 19, 20, (A AND B) NOT PRESENT.

6 T 6

Figure 7-1. Logic Card Detail

The pins of each card connector are arranged in two columns (A and B) and are numbered from the top starting with pin 1 and continuing through pin 14 on the half-size card. The pins of the full-size card are numbered 1 through 34, however pins 18A, 18B, 19A, 19B, 20A, and 20B are omitted.

The logic chassis wire wrap surface (side opposite surface where cards are installed) contains wire wrap pin identification information adjacent to each chassis row. Wire wrap pins are numbered 1 through 17 in each chassis row. When a full-size card (spans two logic rows) is installed in the logic chassis, card connector pins (sockets) 1A and 1B mate with wire wrap pins 1A and 1B of the upper row, while card connector pins 21A and 21B mate with wire wrap pins 1A and 1B of the row immediately below. The logic diagrams for this unit show connections in terms of wire wrap pins.

Test Points

Test points are located near the edge of the card opposite the connector and in other strategic places on the component side of the board. Test points are identified alphanumerically starting with A on the top, outer edge. In most cases, test points A and Z are available for ground reference.

USE OF RELATIVE LEVEL INDICATORS

The relative level indicator is a small circle located at the origin or termination of a signal line, and tangent to a logic symbol. The presence or absence of this indicator tells the conditions that are necessary to satisfy the function of the logic symbol. The presence of the circle indicates a 0 logic level on that line is needed to satisfy the function. The absence of the circle represents a logical 1 as needed to satisfy the function.

The relative level indicator depicts the occurrence of inversion. Figure 7-2 shows some representative examples of the relative level indicator being used in this manner.

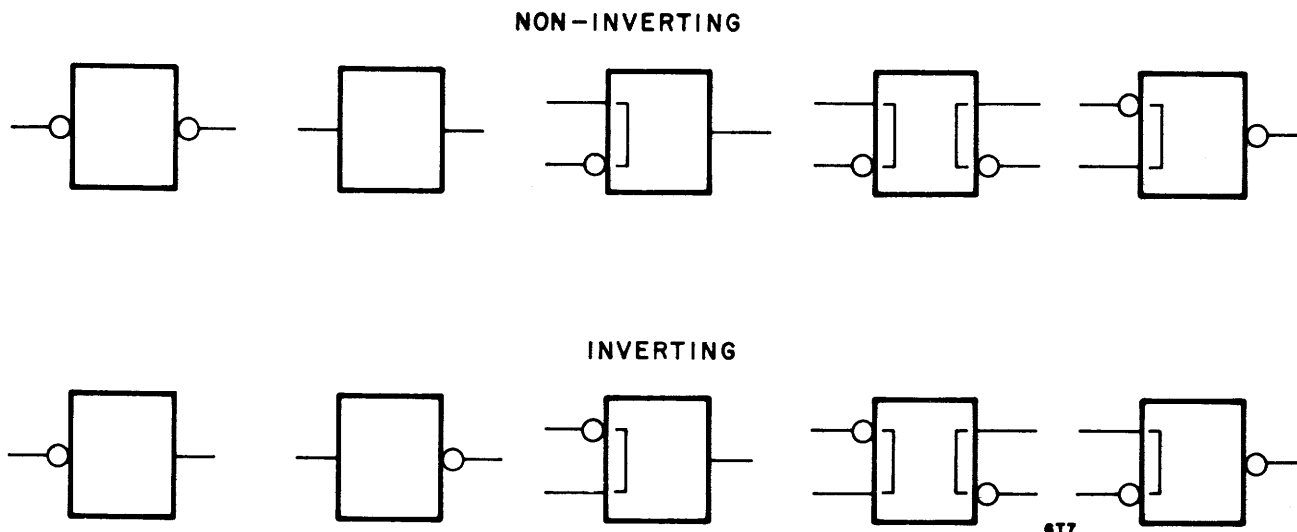


Figure 7-2. Inversion Conventions

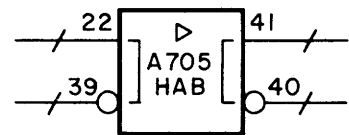
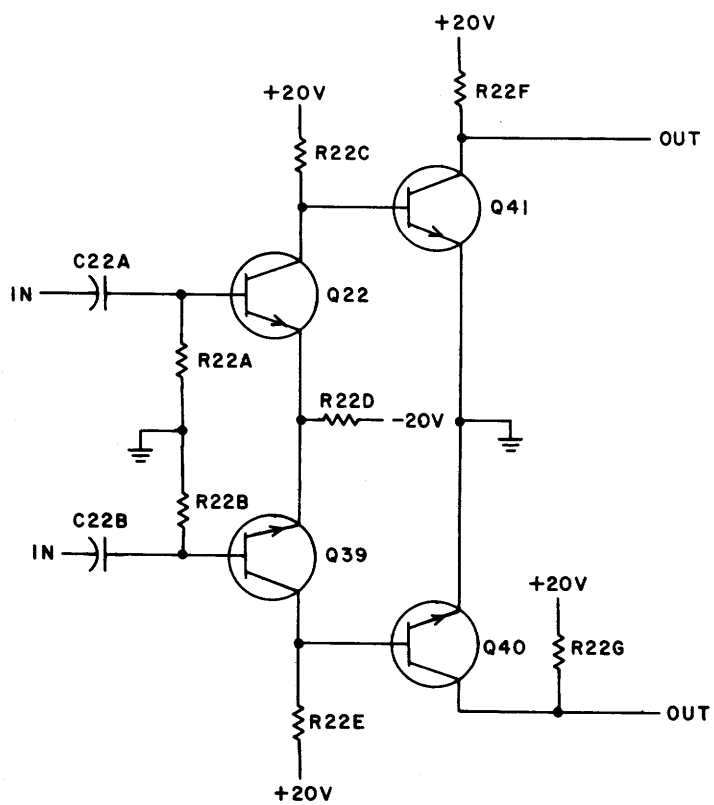
INFORMATION CONTAINED WITHIN LOGIC SYMBOLS

Discrete Component Circuits

Figure 7-3 shows a schematic (as shown on card schematic diagram) and the logical representation (as shown on logic diagrams) for the same theoretical discrete component circuit. Four lines of information are contained within the logic symbol. The top line is the function symbol and designates the board logic function of that particular symbol. In this case, \triangleright represents an amplifier, the logic function performed by the circuit. The third line, also an alphabetic code, designates the circuit type being used (HAB). The circuit type is a subdivision of the function identifier (specifically a high level amplifier). By using the circuit type designator, detailed information on that particular circuit can be derived in the following paragraphs (see Discrete Component Circuit Descriptions).

The second line within the symbol is used to differentiate that particular symbol from similar symbols that appear on the logic diagram. It is called the logic term and consists of a one-letter prefix and an assigned identification number (in this case, A705).

The numbers on the input lines to the symbol indicate which transistor is driven by that input line. For example, the upper input has a number 22 on its line, showing that it drives transistor number 22 (ie., Q22 on the card schematic diagram).



678

Figure 7-3. Discrete Component Circuit

The output lines also have numbers associated with them. These numbers indicate which transistor directly feeds the output line. For example, the lower output line has a number 40 above it, indicating that the output from transistor number 40 (Q40 on the card schematic diagram) drives the lower output line.

The lines on the interior of the logic block that bracket both inputs and both outputs show that the input lines and the output lines are differentials. The relative level indicators show that the amplifier does not invert the signal. Slashes on the inputs and outputs show that the signal levels are non-standard.

Integrated Circuits

Figure 7-4 shows the schematic version (as shown on card schematic diagram) and the logical representation (as shown on logic diagrams) for the same representative integrated circuit.

The most apparent difference occurs in the outline shapes for the circuit. The logic drawings use a four sided block to depict all logic circuits. Two lines of information appear in the logic version that do not appear on the schematic block. They are the function symbol which identifies the block as an OR gate and the logic term which provides specific identification for the circuit. Points of similarity include the package pin numbers and the Control Data element number. Refer to Table 7-1 for manufacturers information of the various element numbers.

The last item of information regarding these two representations involves the location code which borrows part of the schematic symbols reference designator. In the reference designator (U-A4B), the U specifies a non-amplifying integrated circuit, the A4 is the circuits board matrix location for the package, and the B indicates the section of the package. (A 140 package is a four section package. Each section is a separate circuit. Sections are identified A through D.) The location code (on logic drawings) borrows the matrix location and additionally specifies the location of the card in the logic chassis: position 5 of row B.

WIRED FUNCTIONS

The logical representation for wired functions is shown in Figure 7-5. These functions are used where circuits have the capability of being combined as an AND or an OR function by having the outputs connected. This is simply a physical connection and no electrical or electronic components are involved. The logical interpretation of a wired OR function simply requires that one of the inputs be a logic 0 before the output can be a logic 0. The wired AND output will be a logic 1 only when both inputs are logic 1's.

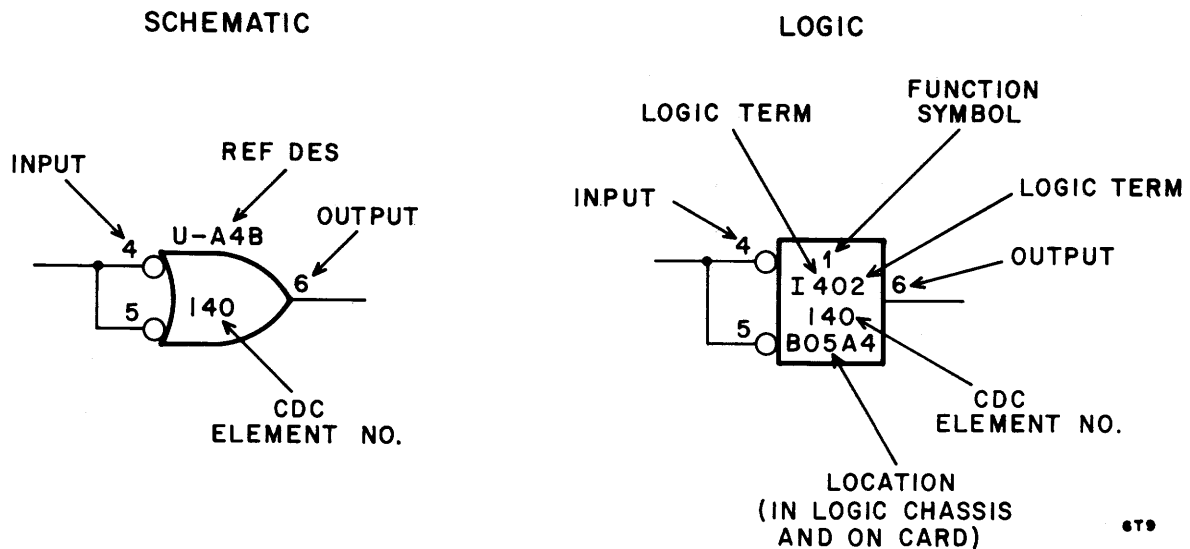


Figure 7-4. Integrated Circuit

TABLE 7-1. CDC ELEMENT NUMBER CROSS REFERENCE

CDC Element No.	Manufacturer, Type	Description
140	Fairchild, 9002	Quad, 2-input NAND
141	Fairchild, 9003	Triple, 3-input NAND
143	Fairchild, 9009	Dual, 4-input buffer
145	Fairchild, 9005	Dual, AND/OR inverter
146	Fairchild, 9016	Hex, inverter
147	Fairchild, 9007	8-input NAND
149H	Motorola, 3021	2-input exclusive OR
161	Fairchild, 9601	Retriggerable multivibrator
162	Texas Instrument, 75107	Dual differential receiver
163	Signetics, 8281	4-bit presettable counter
172H	Motorola, 3002	Quad, 2-input NOR
173H	Motorola, 3004	Quad, 2-input NAND
175	Motorola, 3060	Dual type-D flip-flop
182	Signetics, 8291 or Texas Instrument, 74197	4-bit presettable counter
191	Fairchild, 9301	1 of 10 decoder
200	Texas Instrument, 7406	Hex, inverter
300	Fairchild, 709	Operational amplifier
301	Fairchild, 741	Operational amplifier
304	Fairchild, 715	Operational amplifier



6T10

Figure 7-5. Wired Functions

STANDARD/NON-STANDARD LOGIC LEVEL INDICATOR

The input to a logic function at a voltage other than the standard logic level is represented by a slash across the non-standard level line. Absence of the slash (or absence of an X, see below) indicates a standard logic level on that line.

When the input signal to a logic function is an analog signal, the input line will have an X across it. The analog designator is used on lines that normally operate at more than two voltage levels.

INTEGRATED CIRCUIT DESCRIPTIONS

Basic functional information for integrated circuits is provided on the Key to Logic Symbols sheet of the logic diagrams.

Detailed functional descriptions and schematic diagrams for integrated circuits is available in the circuit manufacturers handbook, Table 7-1.

DISCRETE COMPONENT CIRCUIT DESCRIPTIONS

Figures 7-6 through 7-69 are the schematic diagrams for the discrete component circuits used in this device. A verbal description supports each circuit diagram. The order of presentation is in accordance with the 3-letter alphabetical circuit type designator.

Gated Amplifier - FAB

The FAB circuit (Figure 7-6) is a low level amplifier that amplifies the analog read signal from the head. Input B is a gate input.

When input B is +20v, diodes CRNA, CRNB, CRNC, CRND, CRNE and CRNF are forward biased. The voltage between CRNC and CRNE and between CRND and CRNF is clamped at approximately +2.0v. With all diodes forward biased, the read signal can pass to the amplifier.

When input B is ground, diodes CRNG and CRNH clamp the voltage at +0.6v. This reverse biases the input diodes. No read signal can enter.

The preamplifier is a three stage amplifier using an emitter follower output stage for low output impedance. The integrated preamplifier has discrete component ac and dc feedback.

AC feedback is provided by CNE and RNH in the top half and CNF and RNJ in the lower half of the circuit. The signal is brought back to the emitters of the input stage to increase input impedance.

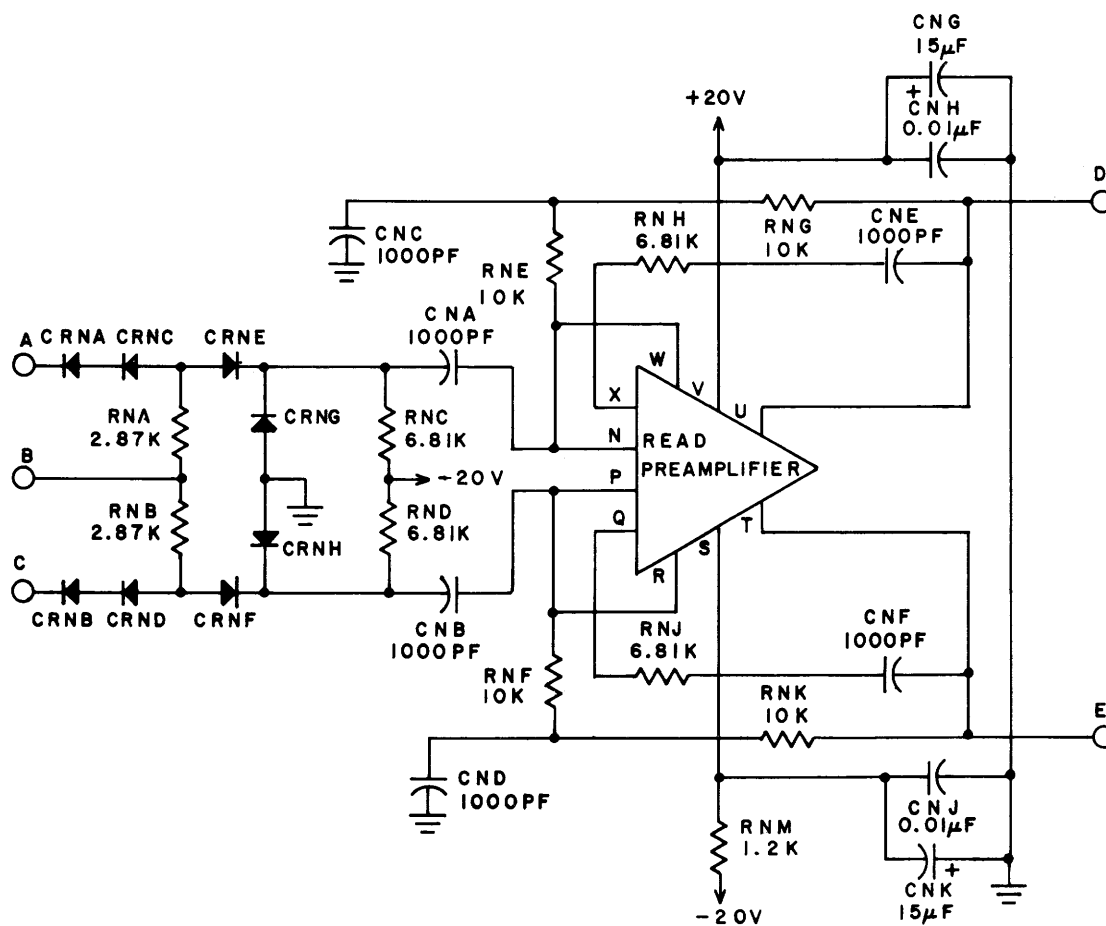
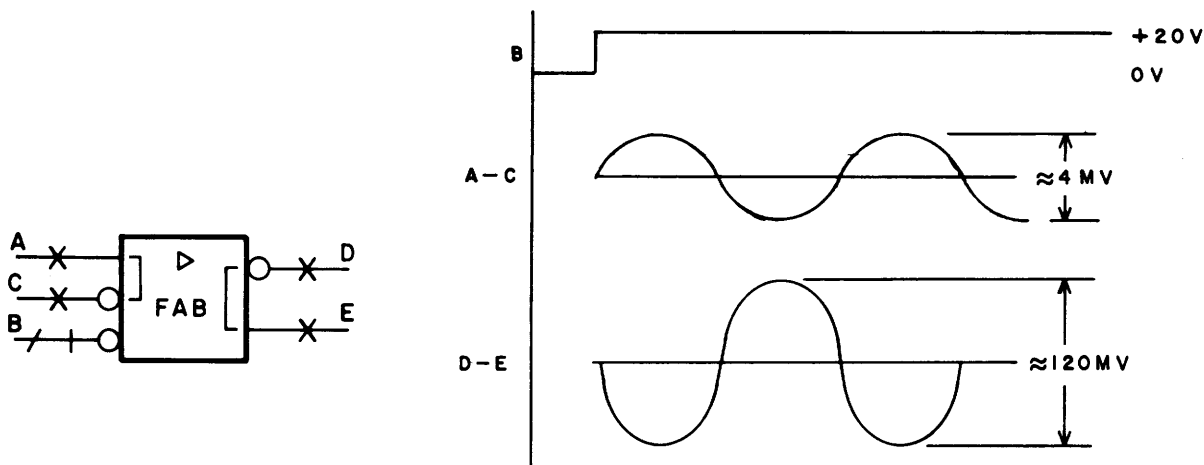
DC feedback is provided by RNG, RNE and CNC (to ground) in the upper half and RNK, RNF and CND (to ground) in the lower half of the circuit. This feedback helps to stabilize the output.

Capacitors CNG, CNH and CNJ, and CNK filter noise from the +20v and -20v power supplies, respectively. The electrolytic capacitors filter low frequency noise. The paper capacitors filter high frequency noise.

Open loop gain in the amplifier is approximately 180. Closed loop gain in the amplifier is approximately 30.

Current Amplifier - FAD

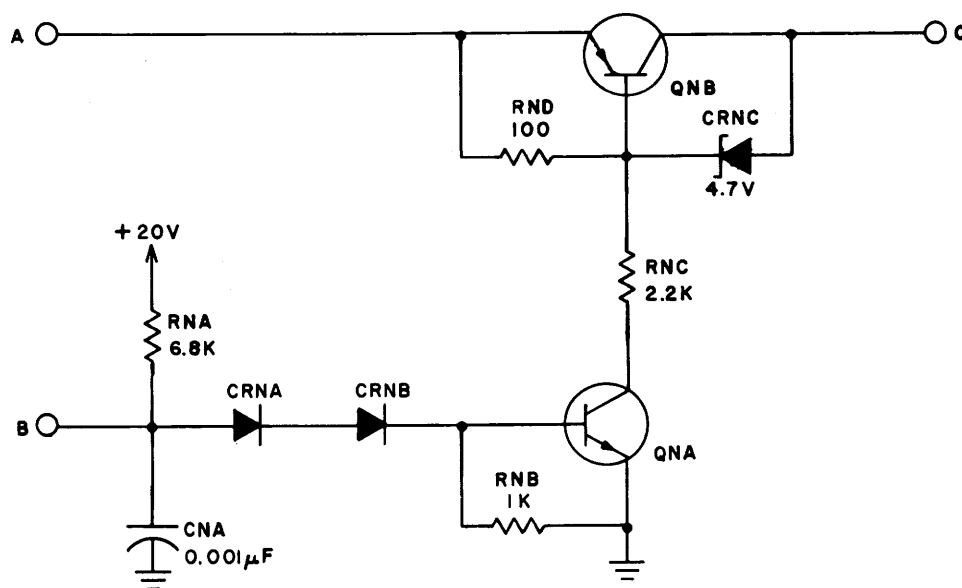
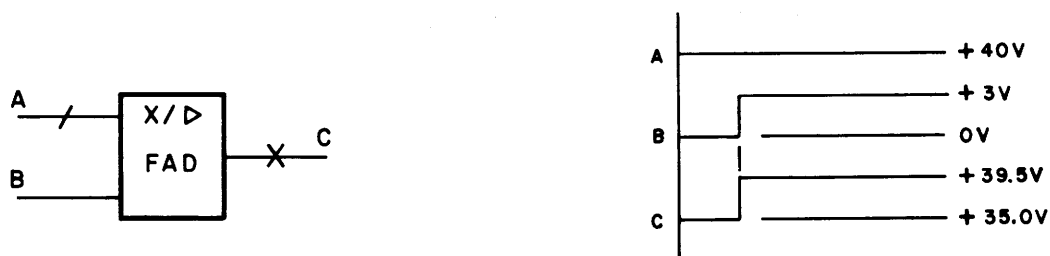
The FAD circuit (Figure 7-7) provides a voltage drop from A to C of either 0.5 or 5.0 volts which is selected with a "1" or a "0", respectively, at B. A "1" at B turns transistor QNA on. This provides base drive through RNC to QNB which turns on. The output at C is now the same as the input at A except for the emitter-collector drop (0.5v) across QNB. With input B at ground, "0", QNA is off and base drive to QNB is provided through the 4.7-volt Zener diode, CRNC. The voltage drop from A to C is V_{be} plus V_z . Resistor RND improves circuit operation by increasing the Zener current.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

6T100

Figure 7-6. Gated Amplifier - FAB



6T101

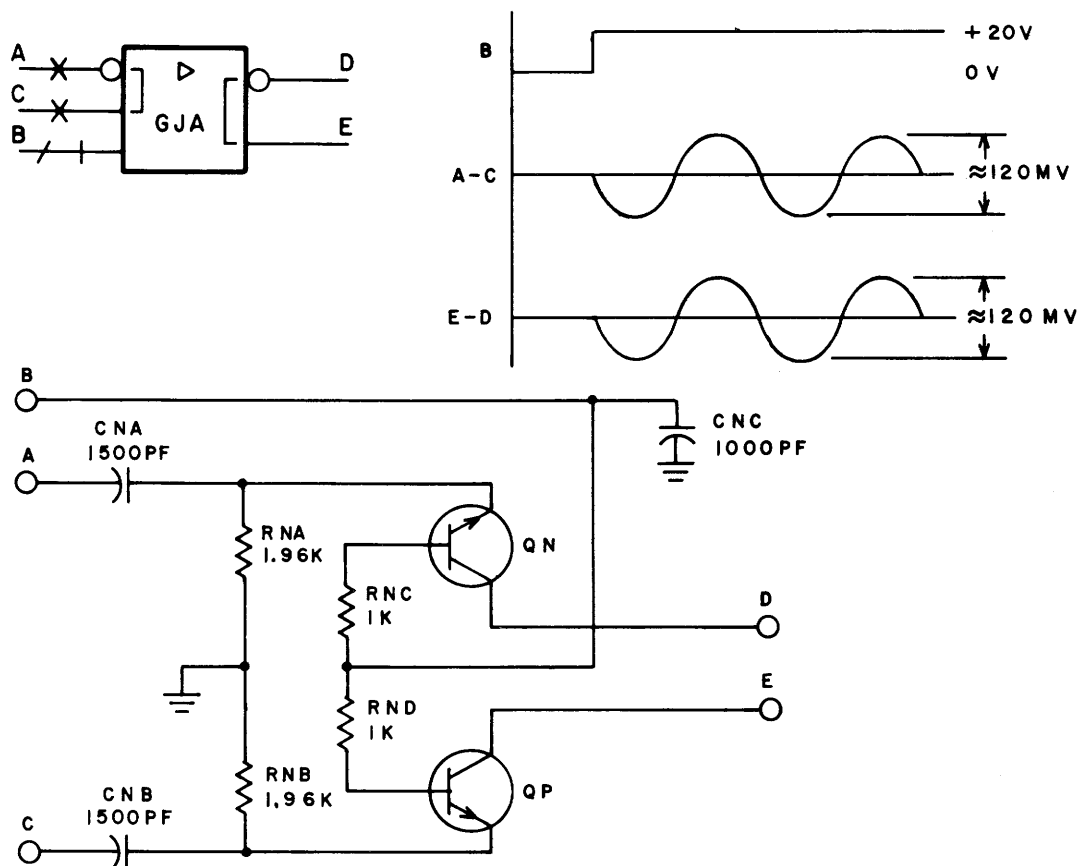
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

Figure 7-7. Current Amplifier - FAD

Gated Intermediate Level Amplifier - GJA

The GJA circuit (Figure 7-8) is an analog gate that is controlled by input B. When input B is +20v, both transistors are on. All analog signals pass through the circuit. Capacitors CNA and CNB ensure that only analog signals are passed. CNC filters noise spikes from the gating signal. Dc power for the transistors is supplied by the circuit in the next stage.

When input B is +0.2v, both transistors are off. No signals pass through the circuit.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

6T102

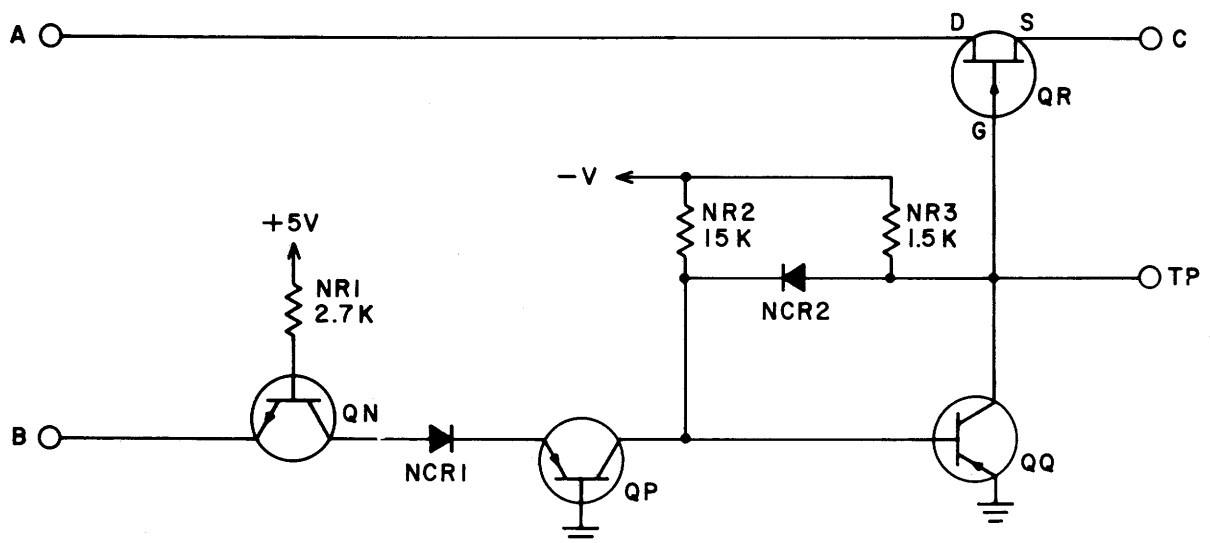
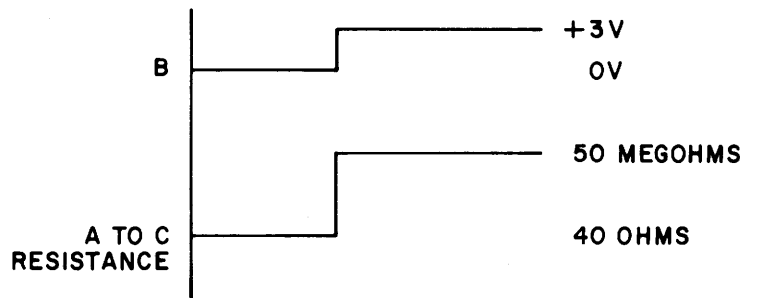
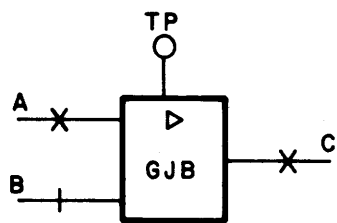
Figure 7-8. Gated Intermediate Level Amplifier - GJA

Gated Analog Clamp - GJB

The GJB circuit (Figure 7-9) functions to turn QR (an N channel junction field effect transistor) on when a logical 0 is applied at input B and to turn QR off when a logical 1 is applied at input B.

In actual application output C is connected to the summing point of an operational amplifier and therefore is always at ground potential. Terminal A is connected to the output of the operational amplifier. When QR turns on, it presents a very low resistance feedback path to the operational amplifier thus forcing the gain of the amplifier toward zero. As a result the operational amplifier is essentially clamped to an output voltage of zero.

The on-off resistances of QR are 40 ohms and 50 megohms respectively.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

6T132

Figure 7-9. Gated Analog Clamp - GJB

Multiple Gate Analog Clamp - GJC

The GJC circuit (Figure 7-10) functions to turn QQ (an N channel junction field effect transistor) on when a logical 0 is applied at any of the B inputs and to turn QQ off when all of the B inputs are at a logical 1.

In actual application output C is connected to the summing point of an operational amplifier and therefore is always at ground potential. Terminal A is connected to the output of the operation amplifier. When QQ turns on, it presents a very low resistance feedback path to the operational amplifier thus forcing the gain of the amplifier toward zero. As a result the operational amplifier is essentially clamped to an output voltage of zero.

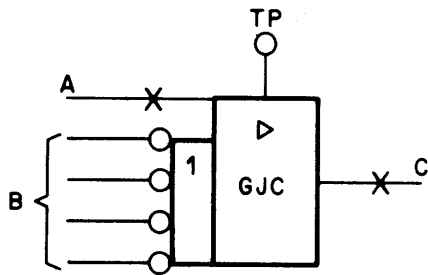
The on-off resistances of QQ are 40 ohms and 50 megohms respectively.

Gated Analog Clamp - GJD

The GJD circuit (Figure 7-11) functions to turn QP (an N channel junction field effect transistor) on when a logical 0 is applied at input B and to turn QP off when a logical 1 is applied at input B.

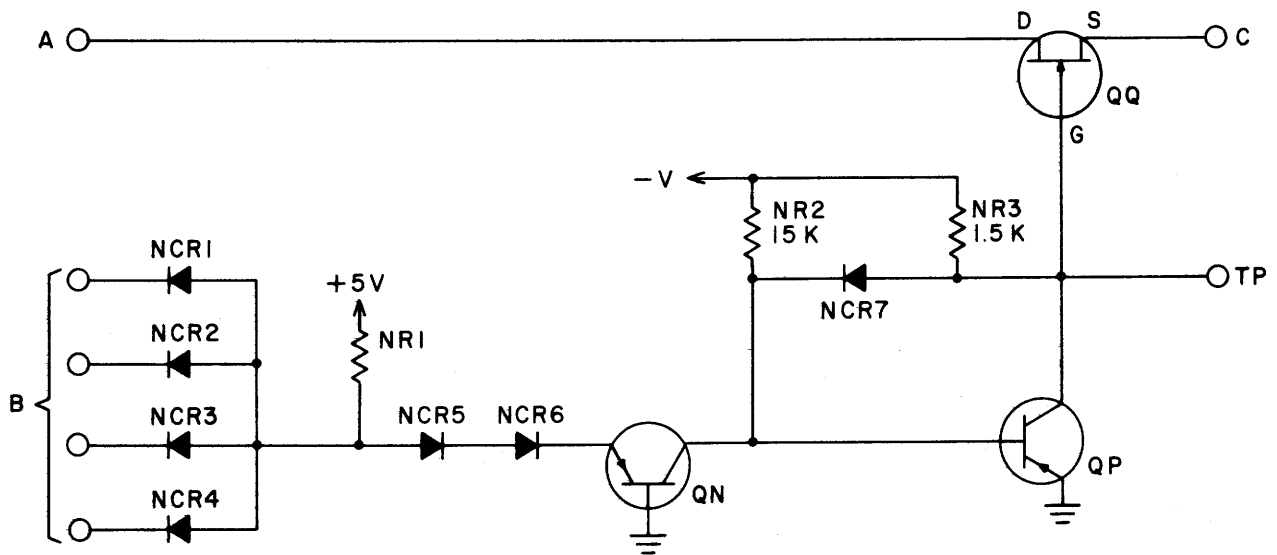
In actual application output C is connected to the summing point of an operational amplifier and therefore is always at ground potential. Terminal A is connected to the output of the operational amplifier. When QP turns on, it presents a very low resistance feedback path to the operational amplifier thus forcing the gain of the amplifier toward zero. As a result, the operational amplifier is essentially clamped to an output voltage of zero.

A series resistor is normally connected between the input analog voltage and point A. The on-off resistances of QP are 40 ohms and 50 megohms respectively.



IF ANY INPUT B EQUALS 0 VOLTS,
THE A TO C RESISTANCE EQUALS 40 OHMS.

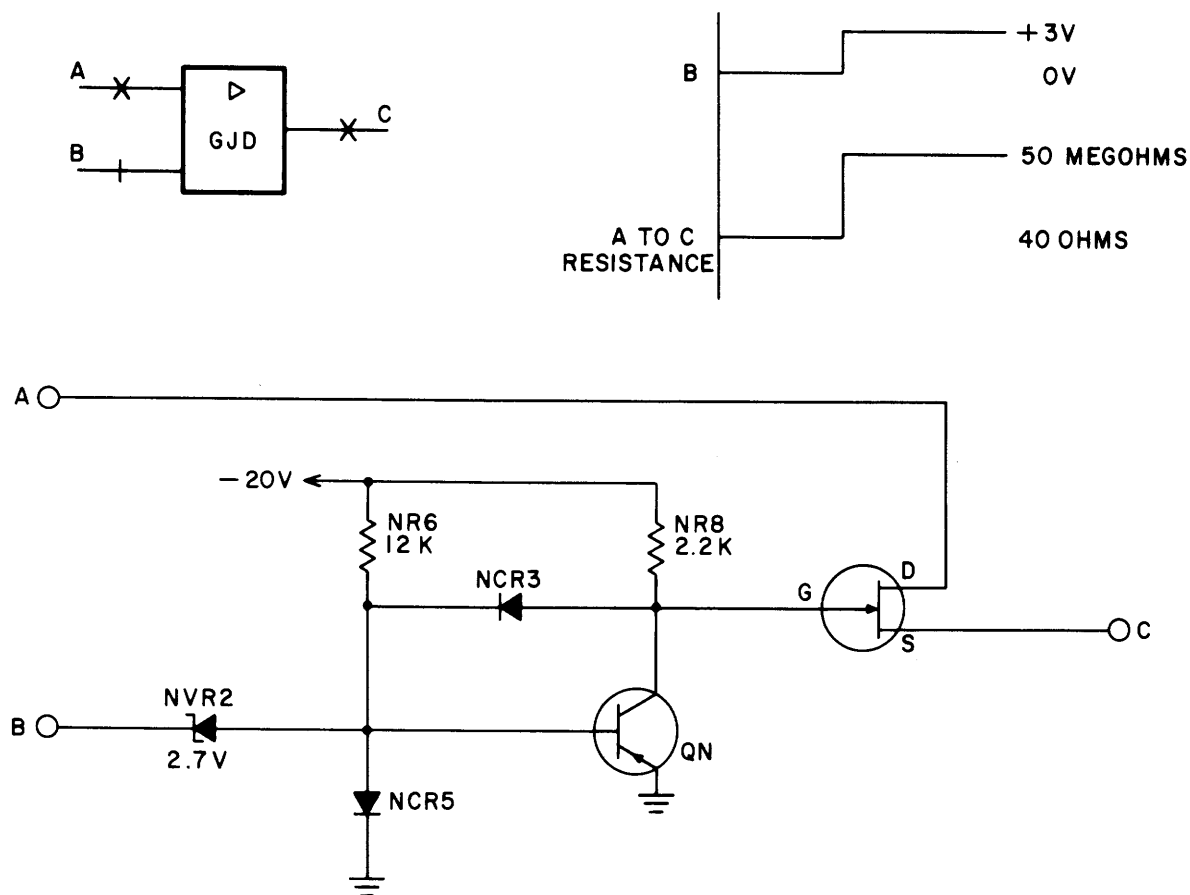
IF ALL INPUT B'S EQUAL +3 VOLTS,
THE A TO C RESISTANCE EQUALS 50 MEGOHMS.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

6T133

Figure 7-10. Multiple Gate Analog Clamp - GJC



6T134

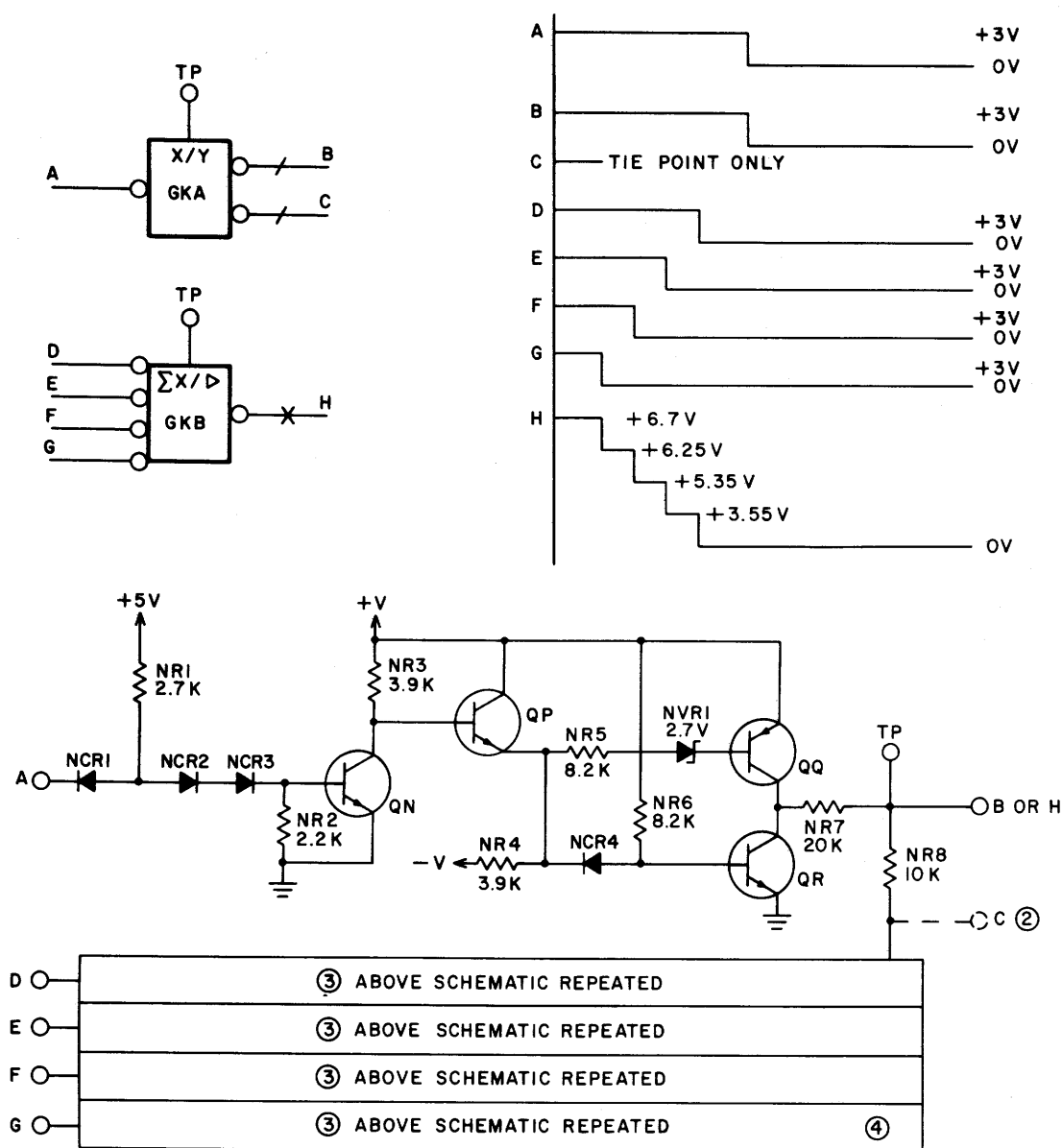
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

Figure 7-11. Gated Analog Clamp - GJD

Level Translator - GKA and Digital to Analog Converter - GKB

The GKA and GKB circuits (Figure 7-12) when used together comprise a 5-bit D/A converter. The GKB circuit used singly is a 4-bit converter.

The GKB consists of four voltage switches and a 4-bit R-2R D/A ladder network. Each voltage switch circuit applies positive voltage to the related ladder input when its input is a logical 1. A voltage switch applies ground to the related ladder network input when its input is a logical 0.



- NOTES: 1. VOLTAGE AND COMPONENT VALUES FOR REFERENCE ONLY.
- ② APPLICABLE TO GKA ONLY.
- ③ APPLICABLE TO GKB ONLY.
- ④ NR8 IN THIS SECTION IS 20K WITH LOWER END TO GROUND.

67135

Figure 7-12. Level Translator and D/A Converter - GKA, GKB

In the GKB circuit, the digital inputs G, F, E, and D are ordered from least to most significant. When all digital inputs are "1's", the voltage at H is +6.7v (assuming a 10k ohm load is provided by the following circuit). When all digital inputs are "0's" the analog output is 0v (except for a +6 mv, max., dc offset). The analog output for an increase of one in the digital input code is +446 mv, nominal.

QN and QP operate as a saturated switch and an emitter follows, respectively, in the voltage switch circuit. QQ and QR operate as low offset saturated switches, only one of which is on at a time.

The R-2R D/A ladder has a resistance of 10k ohms from any node to ground and divides by two the voltage at the next lower, in significance, node.

The GKA circuit is identical to one stage of the GKB.

Level Translator - GKC

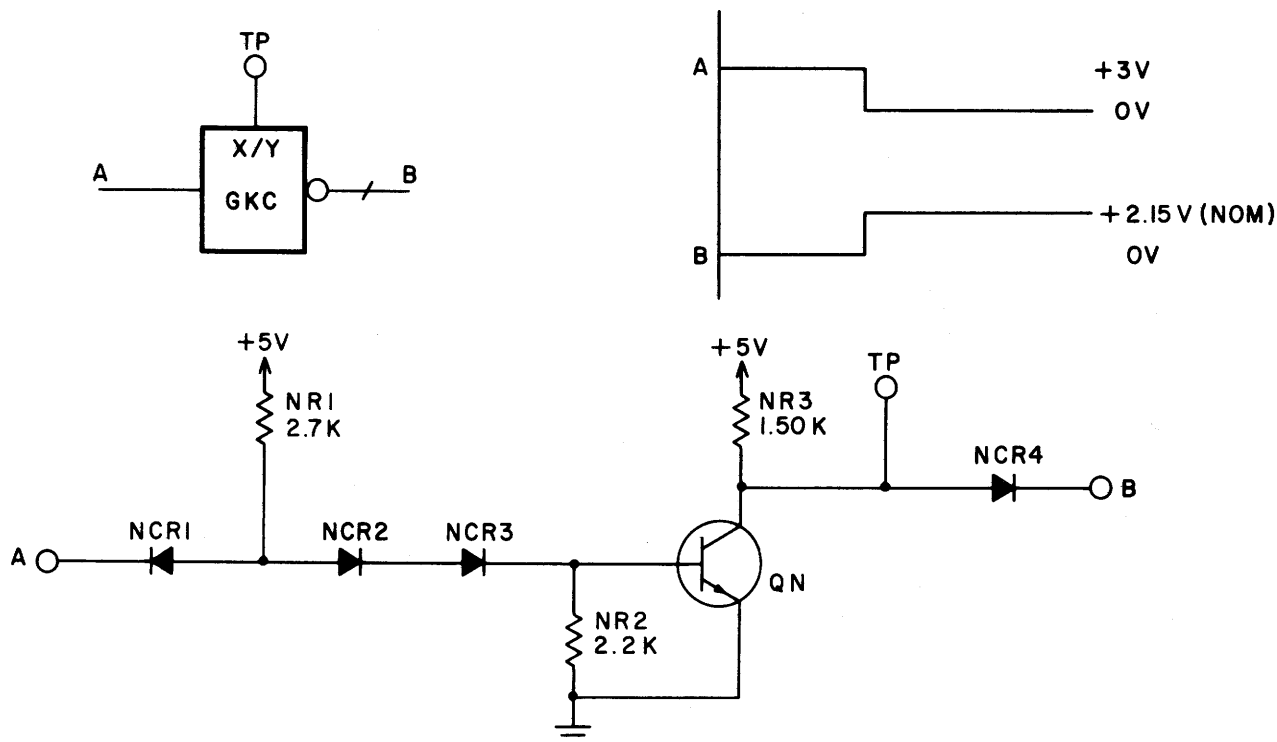
The GKC circuit (Figure 7-13) converts a logical 0 to a +2.15 (nominal) level used to inject a current signal into the summing point of an operational amplifier. Typically a resistor is connected between point B and the operational amplifier summing point to establish the magnitude of this current.

When a logical 1 is present at input A, transistor QN saturates, the output diode NCR4 shuts off, and output B drops to 0 volts removing the current to the operational amplifier summing point.

High Level Amplifier - HAA

The HAA circuit (Figure 7-14) is gated by an analog gate circuit (GJA) and provides the load and biasing for that circuit.

The preamplifier, ac feedback and dc feedback are identical to the FAB circuit. Capacitor CND is added to the output of the second stage to decouple high frequency noise.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

6T136

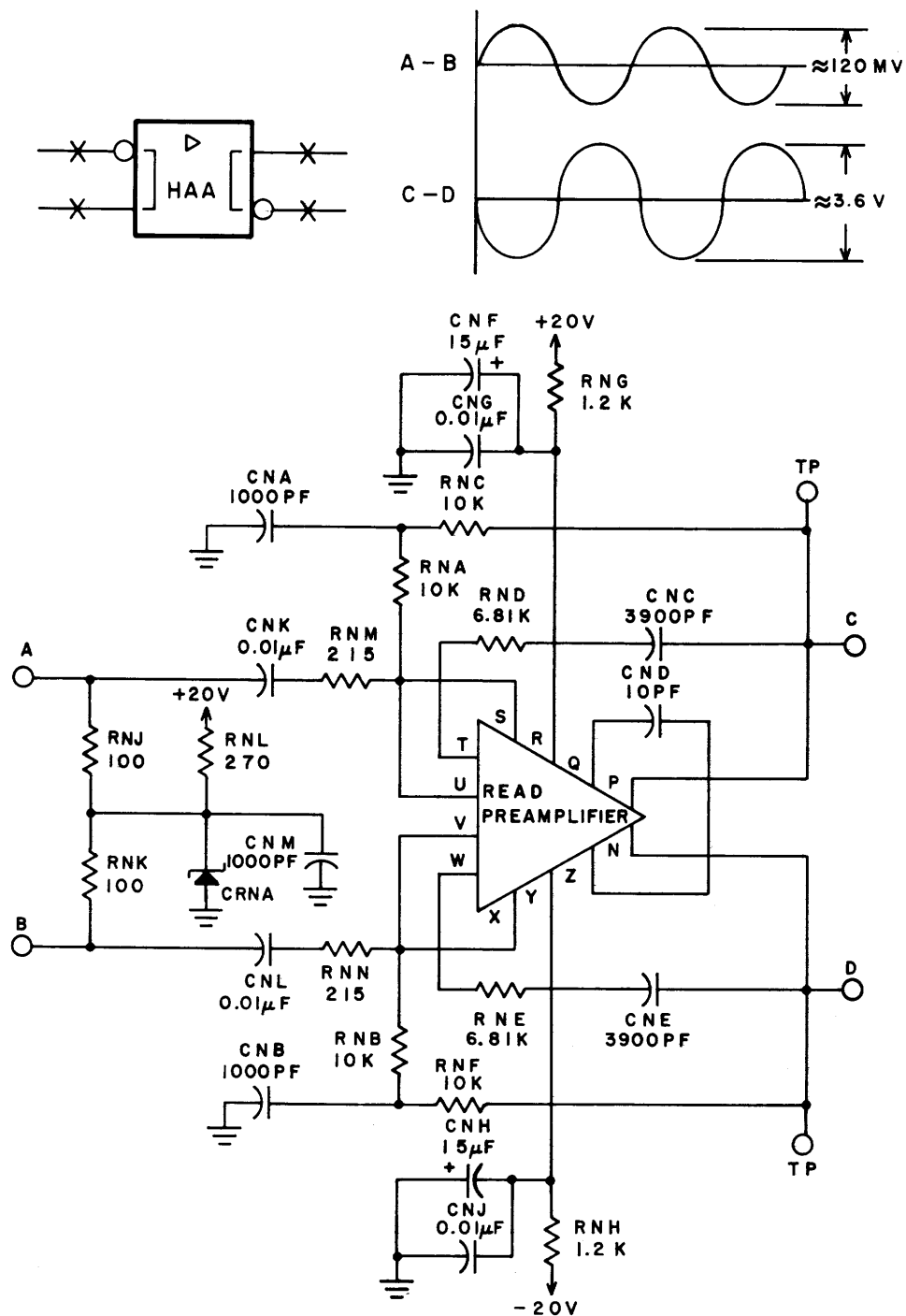
Figure 7-13. Level Translator - GKC

High Level Amplifier - HAB

Input to the HAB circuit (Figure 7-15) is a balanced square wave. Output is also a balanced square wave that follows the input.

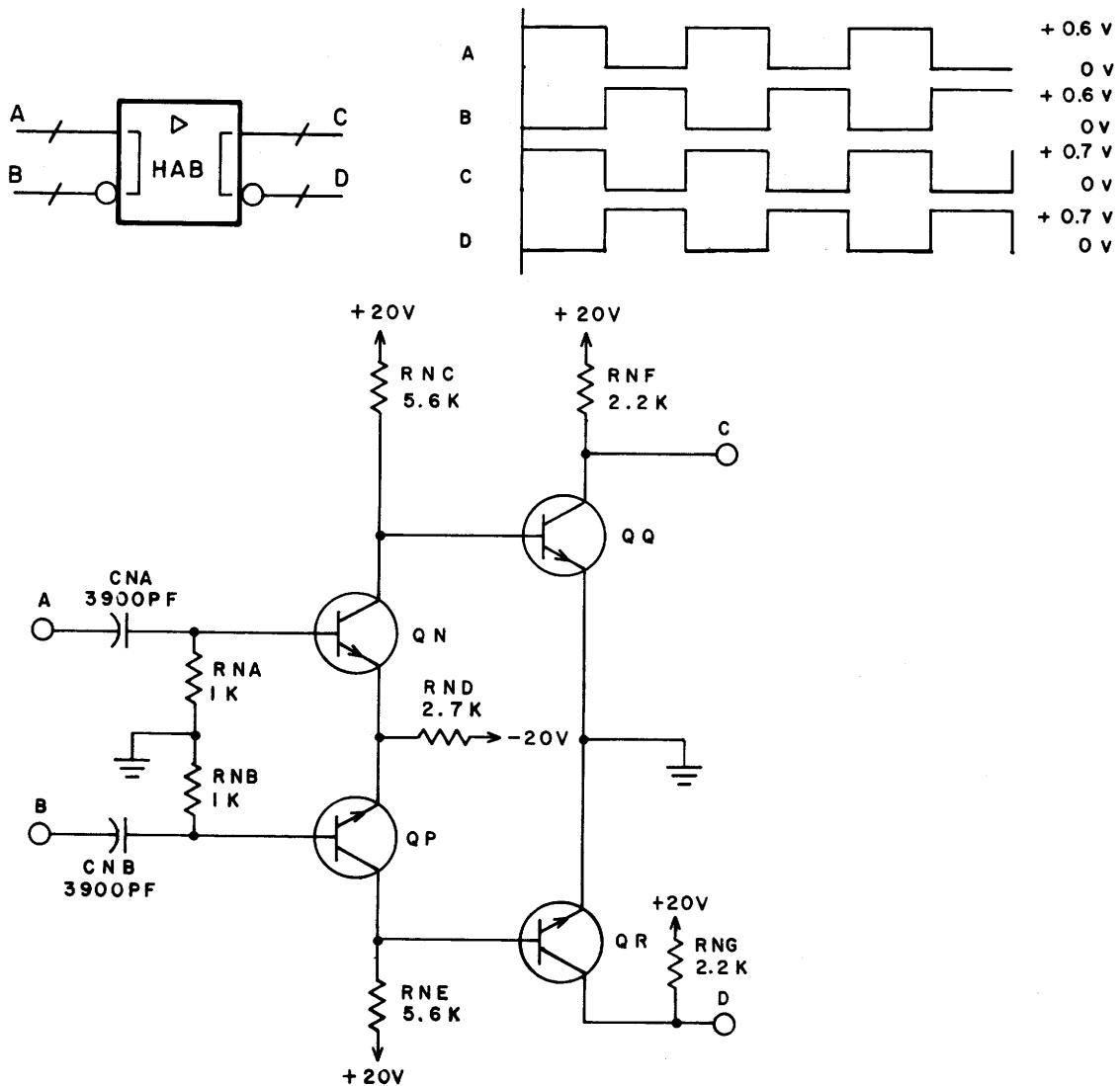
When input A is positive, B is at 0v. Transistor QN is on and QP is off. The base of QQ falls to near ground. Transistor QQ is off. Output C rises to approximately +0.7v. With QP off, QR turns on. Output D falls to ground.

When input B is positive, A is at ground. Transistor QN is off, QP is on, QQ is on and QR is off. Output C is at ground. Output B rises to +0.7v.



6T103

Figure 7-14. High Level Amplifier - HAA



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

6T104

Figure 7-15. High Level Amplifier - HAB

High Level Amplifier - HJA

The HJA circuit (Figure 7-16) increases the input signal power to transmit over a coaxial cable. The input is a differential signal of approximately 3.6v peak to peak.

The input signal across A and B is divided between resistors RNA and RNB. Transistors QN and QP are forward biased with a gain of 3. The -20v through resistor RNH and diodes CRNA and CRNB and through resistor RNJ and diodes CRNC and CRND forward biases QQ and QT, respectively. Transistors QQ and QT are in a common collector configuration to provide a current gain.

Transistors QR and QS are emitter followers that draw very little current from QQ and QT. They provide low impedance for discharging CNC and CND, thus reducing delay time when crossing the zero volt point.

Output voltage is approximately the same as input voltage. Output current is 20 ma maximum.

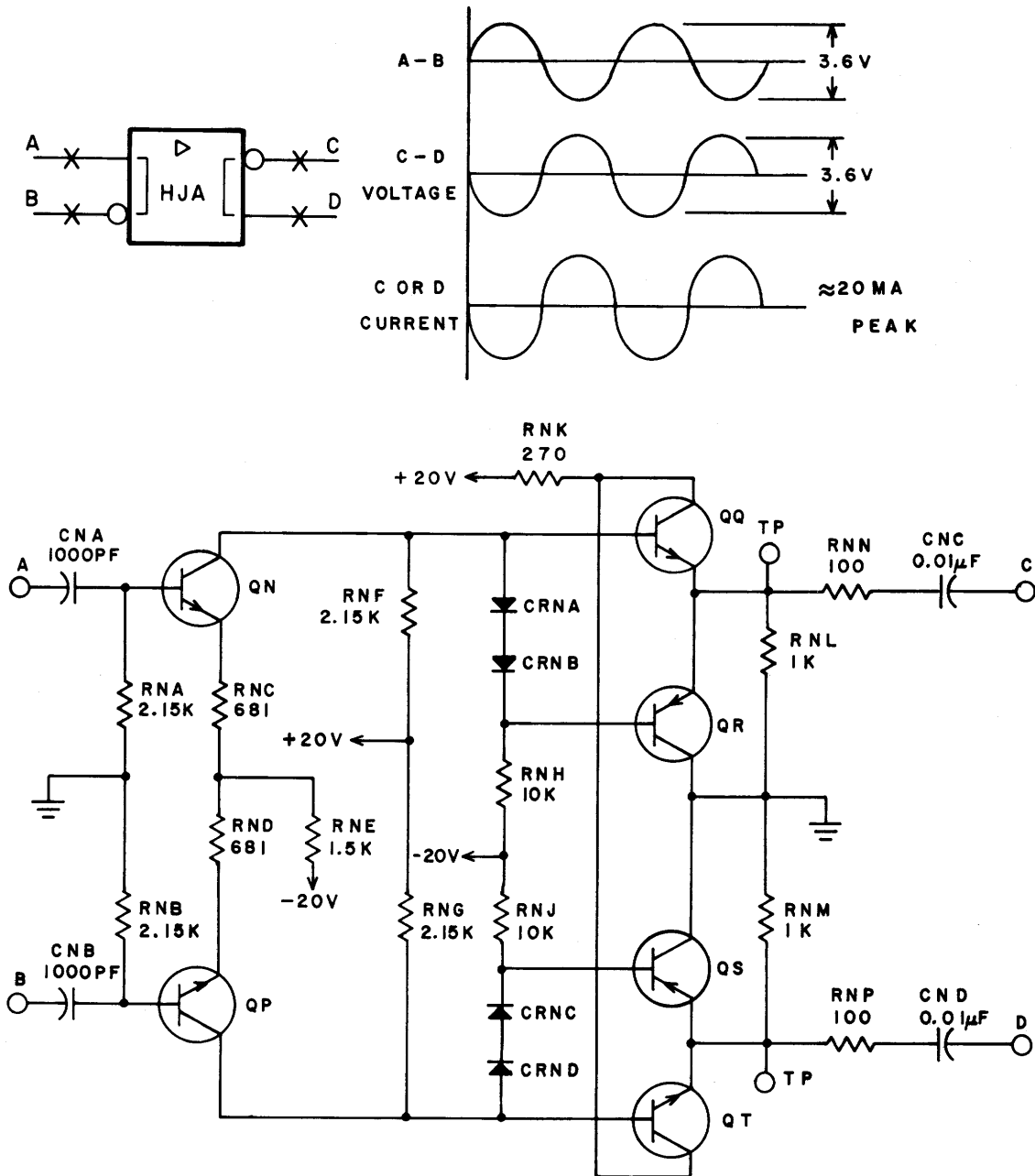
Analog Power Amplifier - HJB

The HJB circuit (Figure 7-17) is designed to have a nominal gain of 1 (after trimming) at a frequency of 50 kHz.

The circuit consists of an input emitter follower (QN), a phase splitter (QP), and a class A quasi-complementary output stage (QQ and QR). Both the input and output are ac coupled.

A trimming resistor, NR2, is selected so that the output amplitude may be established at 15 volts pp.

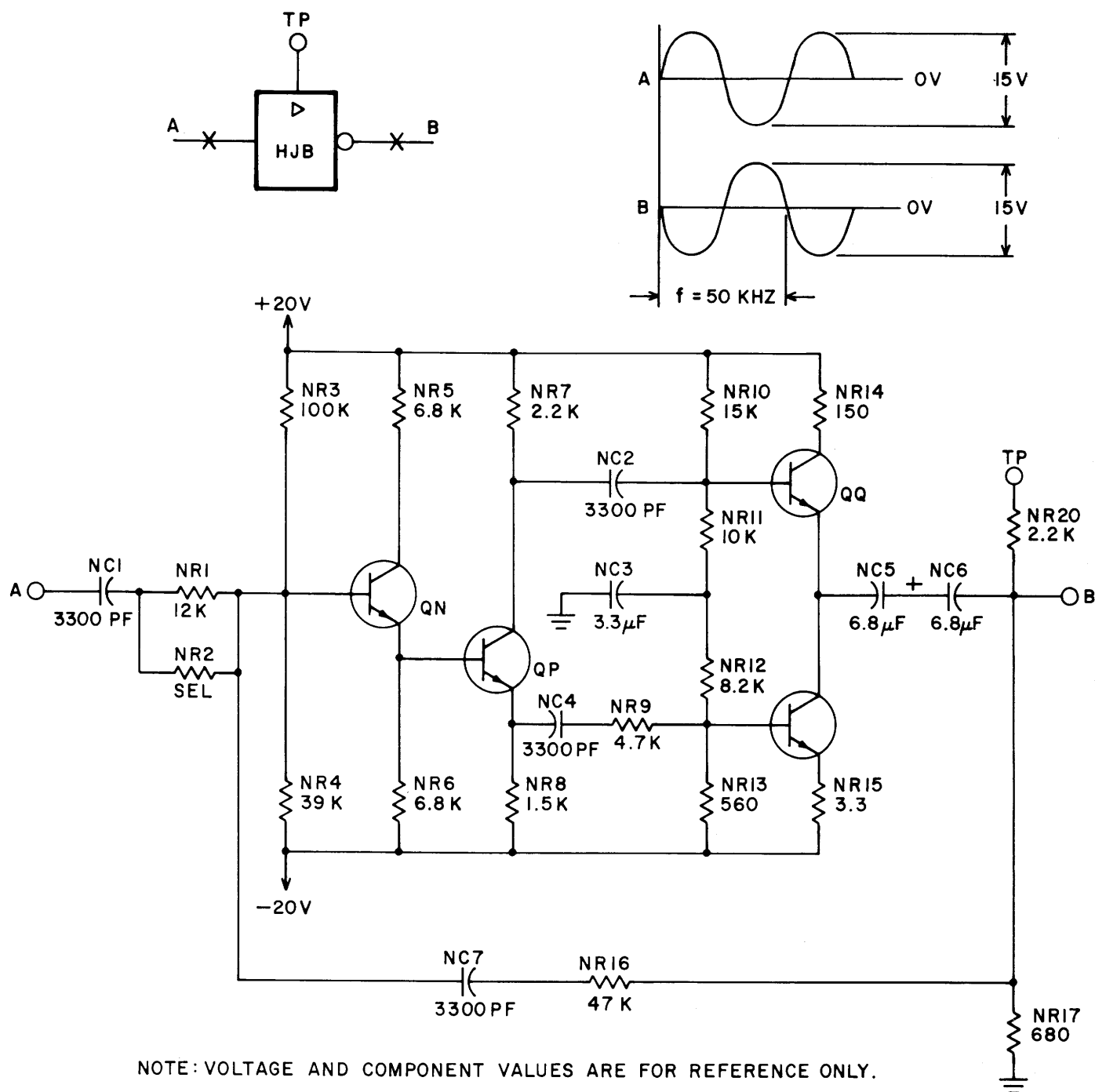
The overall circuit phase shift at 50 kHz is 180 degrees. A negative feedback path (NC7 and NR16) provides circuit stability and gain limiting.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

6T105

Figure 7-16. High Level Amplifier - HJA



6T137

Figure 7-17. Analog Power Amplifier - HJB

Differential Amplifier - HJC

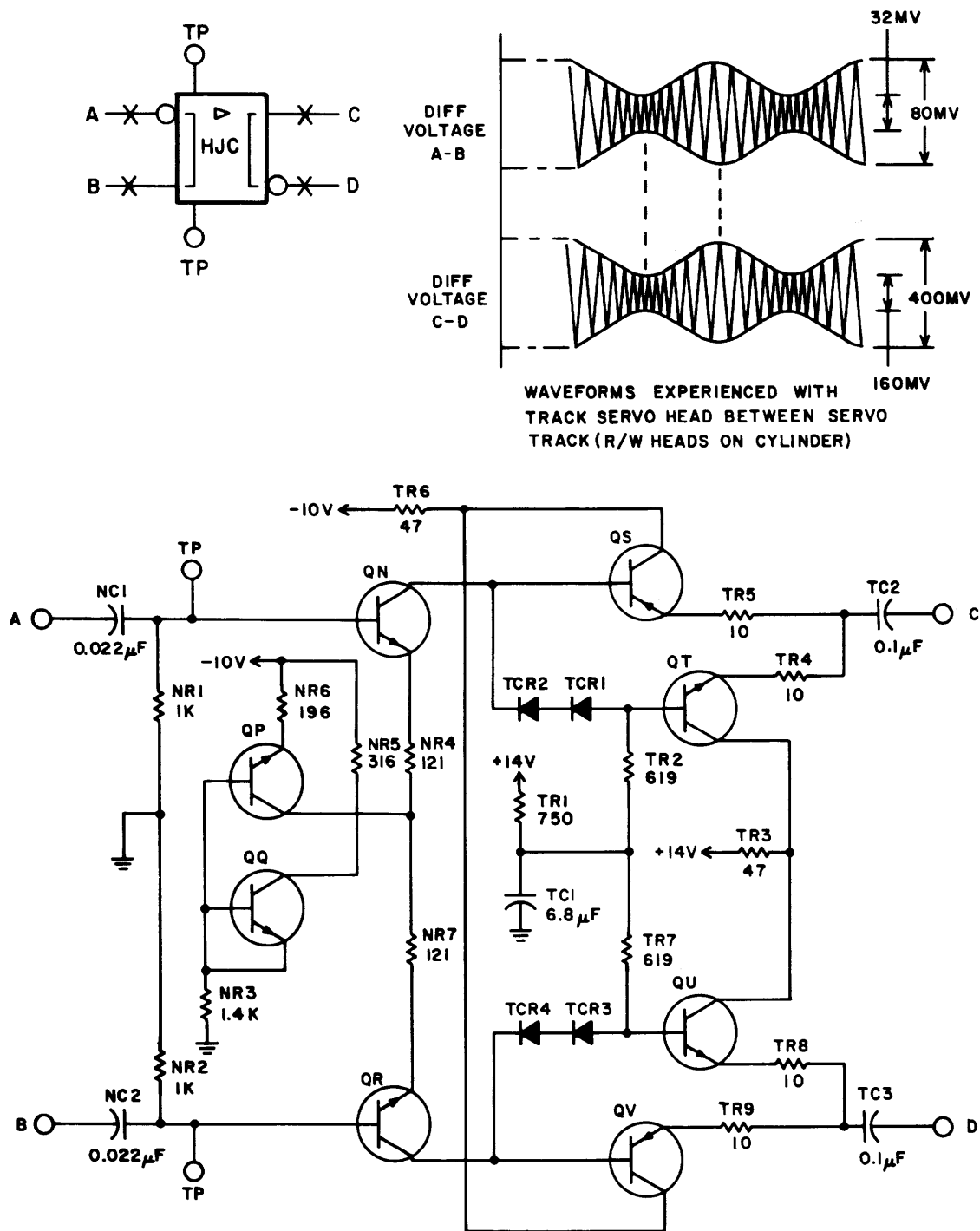
The HJC circuit (Figure 7-18) is a differential amplifier with a voltage gain of 5 (14 db). The input/output waveforms shown on the figure are drawn for a situation where the track servo head is positioned between two tracks (of 406 tracks prerecorded alternately at 455 and 500 kHz) of the track servo disk pack surface. The beating together of the two frequencies causes the signal amplitude changes. The signal at maximum amplitude is an equal mixture of the 455 and 500 kHz frequencies.

Transistors QP and QQ constitute a current source for the differential amplifier. Signal amplification occurs at transistors QN and QR. Transistors QS, QT, QU, and QV are the current buffers for the outputs.

Amplifier/Level Translator - HJD

The HJD circuit (Figure 7-19) is an amplifier that provides a half-wave rectified, shifted output signal.

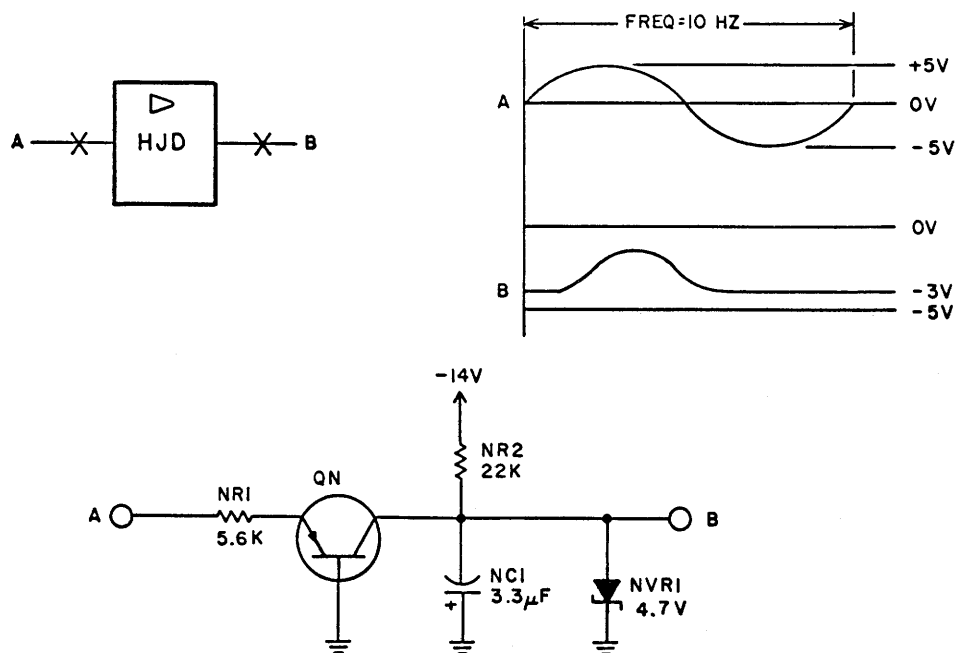
The output signal at B increases in a positive direction from a -3 vdc level. The output signal controls a N-channel JFET in an AGC loop that regulates the amplitude of the fine position servo signal.



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

6T168

Figure 7-18. Differential Amplifier - HJC



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY

6T167A

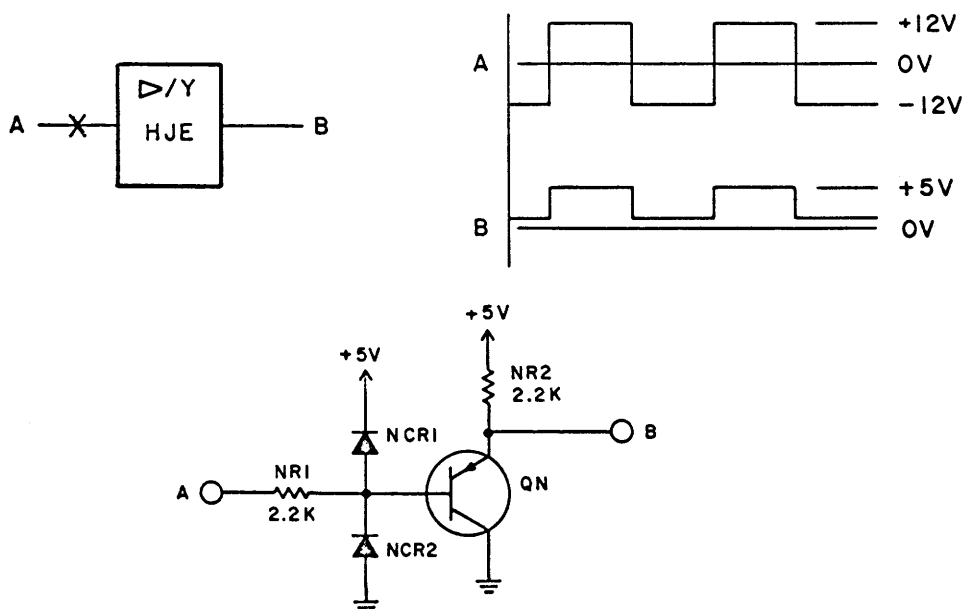
Figure 7-19. Amplifier/Level Translator - HJD

Level Translator - HJE

The HJE circuit (Figure 7-20) converts the output of an operational amplifier to a standard logic level.

When input A is at -12 volts, transistor QN is on. Diode NCR2 limits the input voltage at the base of QN to approximately -0.7 volt. Since the base to emitter voltage of QN is +0.8 volt, output B is at a level of approximately +0.1 volt.

When input A switches to +12 volts, QN becomes reverse biased and output B approaches +5 volts. The base voltage of QN is limited to approximately +5.7 volts by diode NCR1.



NOTE:

VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

6T166A

Figure 7-20. Level Translator - HJE

Differential Amplifier - HJF

The HJF circuit (Figure 7-20.1) is a differential amplifier with a voltage gain of 5 (14 db).

Signal amplification occurs at transistors QN and QP. Transistors QQ and QR are the current buffers for the outputs.

Differential Amplifier - HJG

The HJG circuit (Figure 7-20.2) is a differential amplifier with a voltage gain of 13 (22.3 db).

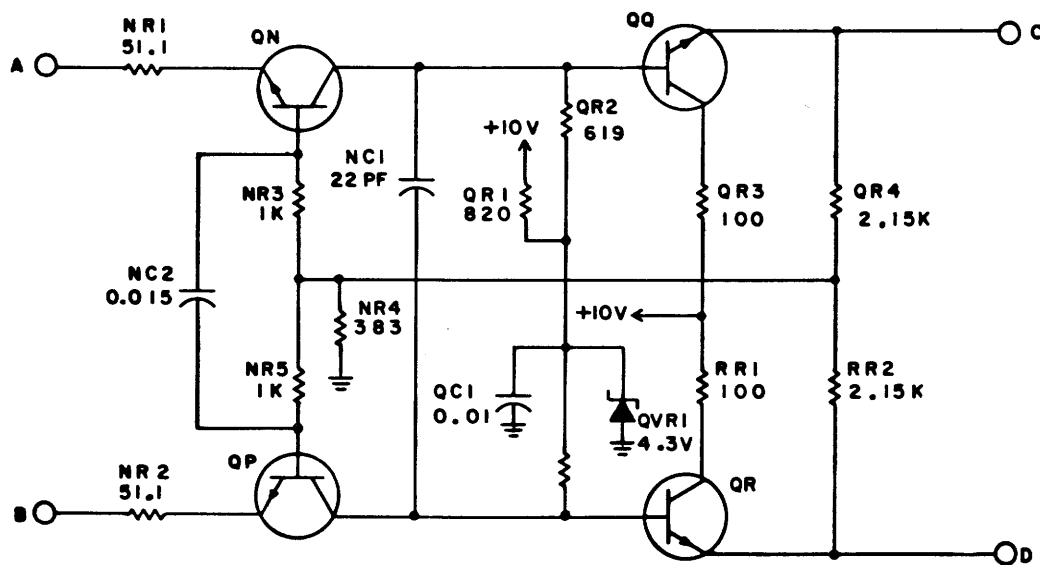
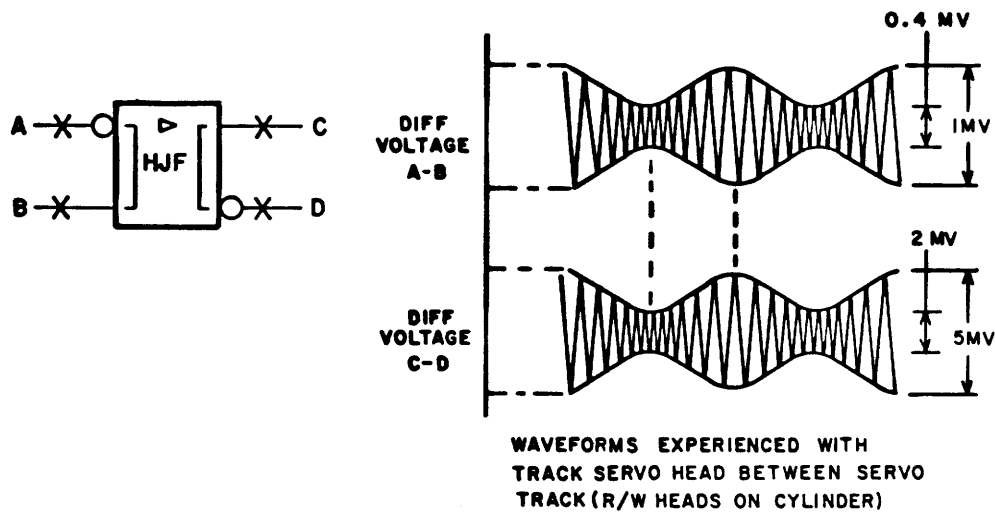
Transistors QP and QQ constitute a current source for the differential amplifier.

Signal amplification occurs at transistors QN and QR.

Transistors QT and QS are the current buffers for the outputs.

Differential Amplifier - HJH

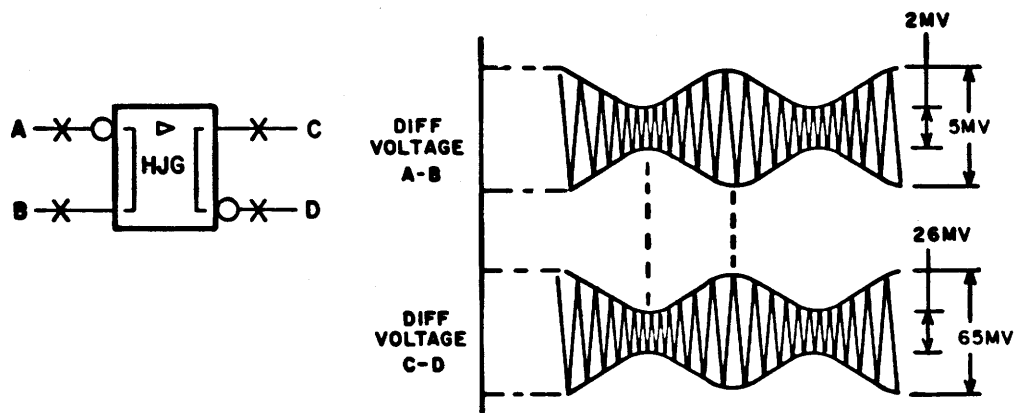
The HJH circuit (Figure 7-20.3) is a differential amplifier with a voltage gain of 5 (14 db). The input/output waveforms shown on the figure are drawn for a situation where the track servo head is positioned between two tracks (of 406 tracks prerecorded alternately at 455 and 500 kHz) of the track servo disk pack surface. The beating together of the two frequencies causes the signal amplitude changes. The signal at maximum amplitude is an equal mixture of the 455 and 500 kHz frequencies.



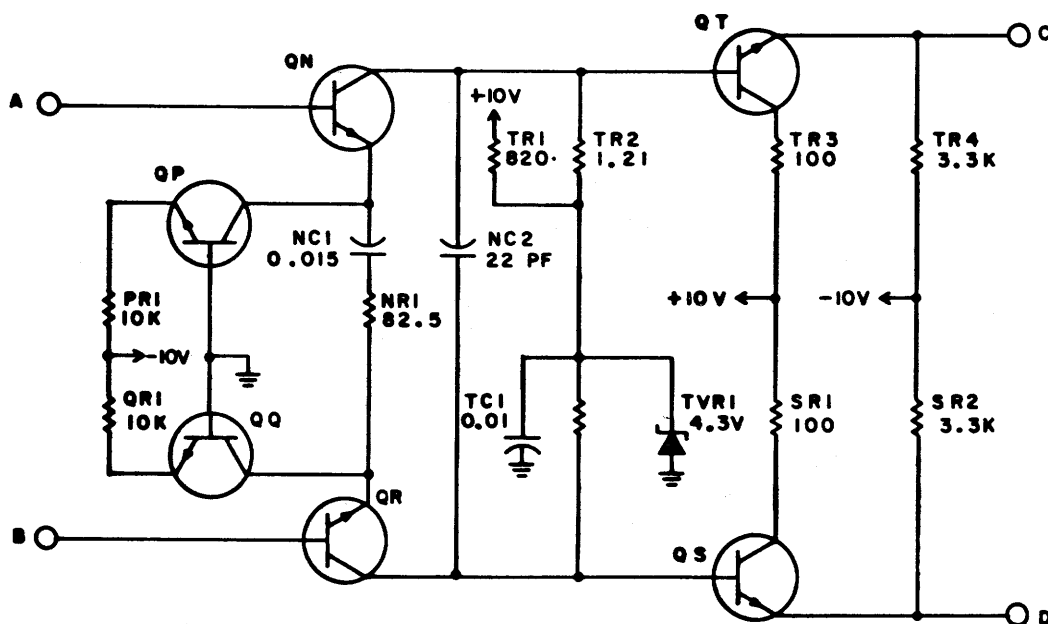
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

6T170

Figure 7-20.1. Differential Amplifier - HJF



WAVEFORMS EXPERIENCED WITH
TRACK SERVO HEAD BETWEEN SERVO
TRACK (R/W HEADS ON CYLINDER)



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

6T171

Figure 7-20.2. Differential Amplifier - HJG

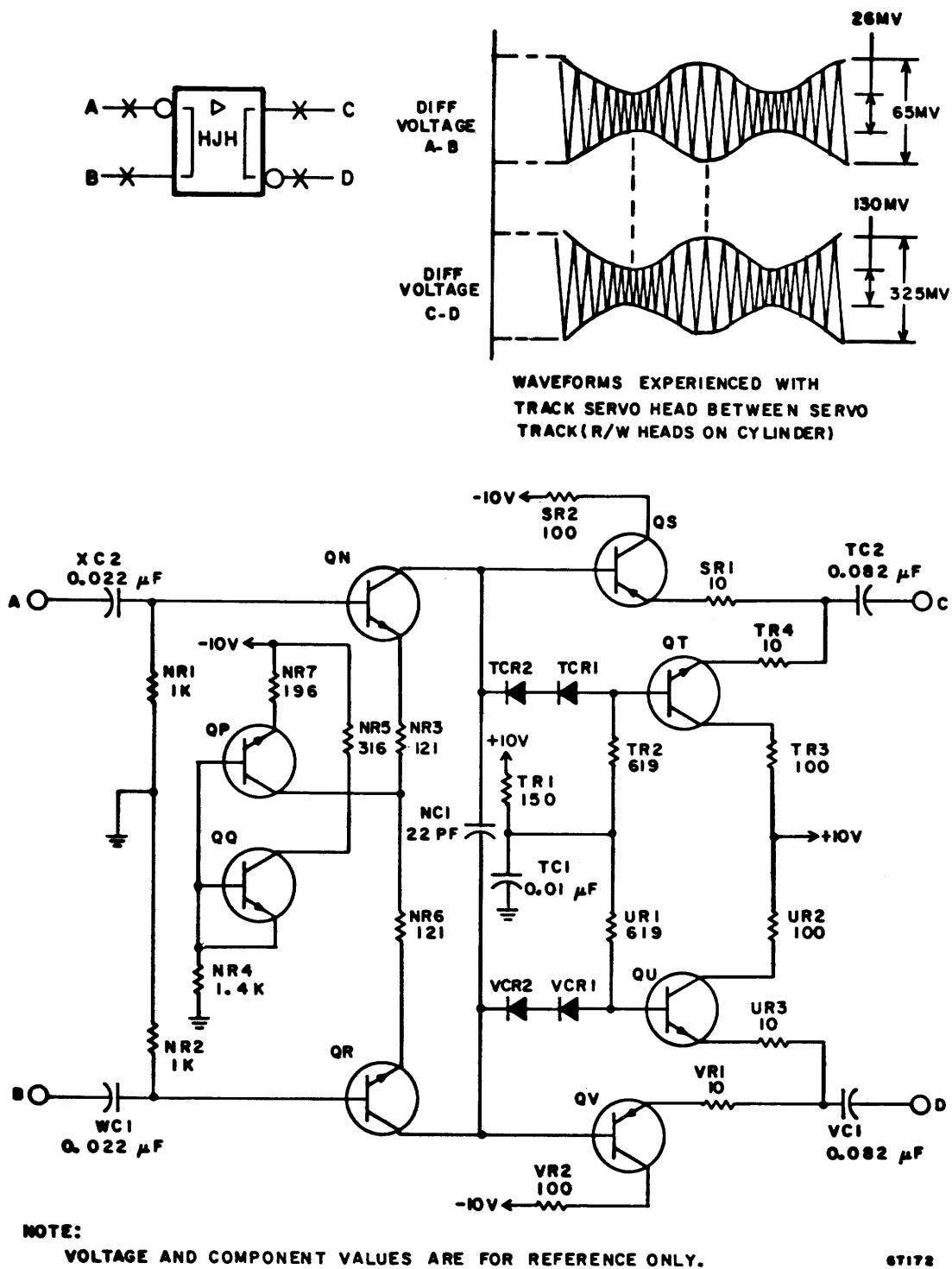
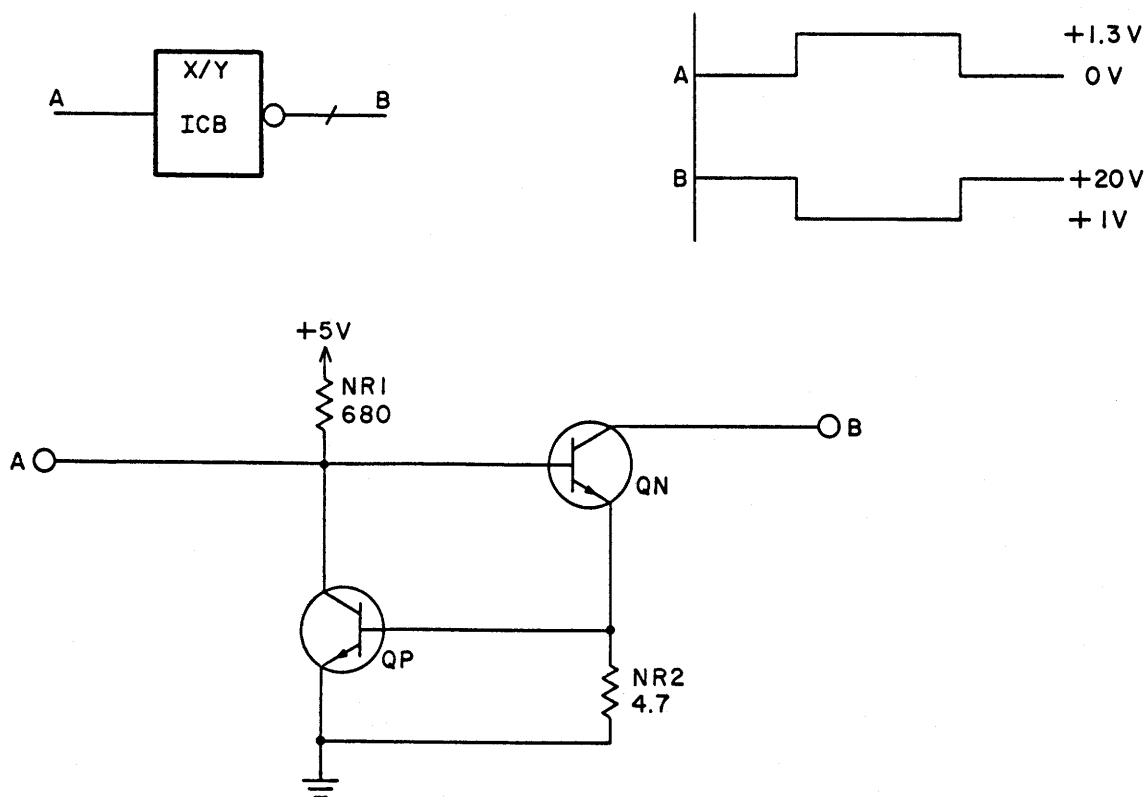


Figure 7-20.3 Differential Amplifier - HJH



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

ST148

Figure 7-21. Lamp Driver - ICB

Lamp Driver - ICB

The ICB circuit (Figure 7-21) drives a lamp which terminates at +20 volts. The circuit is (and must be) driven by an open collector integrated circuit. The nominal current of the lamp must not exceed 100 ma.

QP and NR2 serve as a current limiter. When approximately 140 ma flows through NR2, QP turns on and diverts base current from QN to ground. This prevents surge currents of greater than 140 ma.

When a high, logic 1, is provided to the circuit input, transistor QN (and the lamp) turns on.

A low (logical 0) at the input turns QN off causing the circuit output to rise to the lamp termination voltage. With no path to ground available, the lamp turns off.

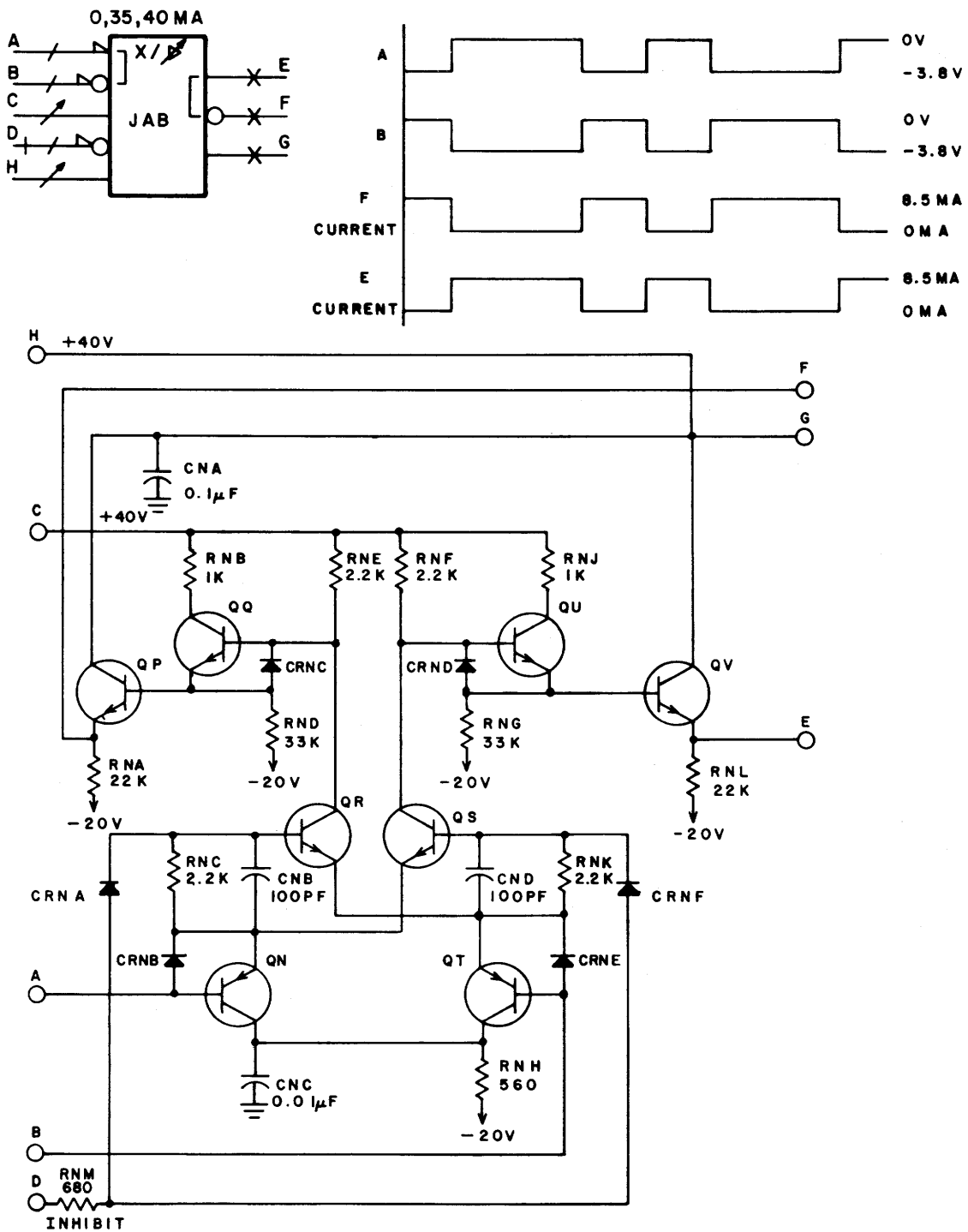
Write Driver - JAB

The JAB circuit (Figure 7-22) provides current to the write heads so that data may be recorded. Outputs E and F are connected to opposite ends of the write head, which is center tapped to ground. When input A is positive, current flows through output E to its half of the write head. When input B is positive, current flows through output F to its half of the write head. When A is positive and the unit is writing, B is negative. When A is negative and the unit is writing, B is positive. Therefore, only one half of the write head may be activated at any one instant while the unit is writing.

With a positive charge on input A, transistor QN is off. The base of QR is positive and the emitter of QS is positive. The negative voltage at B turns transistor QT on. This drives the emitter of QR negative. Transistor QR conducts, driving the base of QQ to about -2v. Transistor QQ is an emitter follower, so the emitter of QQ is also near -2v. The -2v on the base of QP turns QP off. No current flows through output F (-20v through resistor RNA only reverse biases an external diode). With QT on, the base of QS goes slightly negative. Transistor QS is off, allowing the base of QU to go to +40v. Transistor QU is an emitter follower, so the emitter of QU also goes to about +40v. The +40v on the base of QV turns QV on. Current now flows from a +40v supply connected to output G through transistor QV and its half of the write head to ground. A resistor lies between output E and the write head to limit the current flow in the write head.

When input A goes negative and B goes positive, QN and QS are on and QR and QT are off. On the bases of QQ and QU are currents of +40v and -2v, respectively. The emitter of QQ goes to about +40v. The emitter of QU goes to about -2v. Transistor QV is off. No current flows through output E. Transistor QP is on. Current flows from the +40v source connected to output G through QP and its half of the write head to ground.

Input D supplies a negative voltage when the unit is writing to reverse bias diodes CRNA and CRNF. If the unit is not writing, D is grounded and both inputs A and B go negative. This turns on QR and QS. Transistors QP and QV are, therefore, off and no current flows through the write head.



6T108

Figure 7-22. Write Driver - JAB

Write Driver - JAD

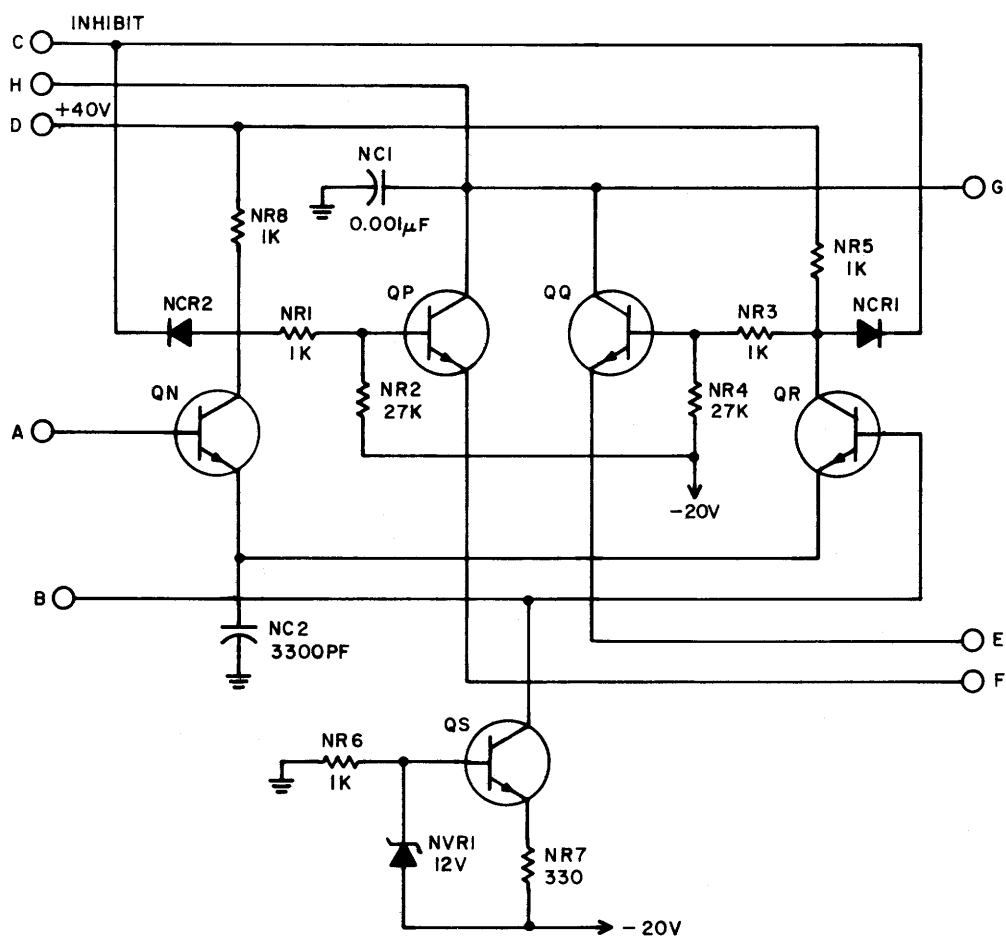
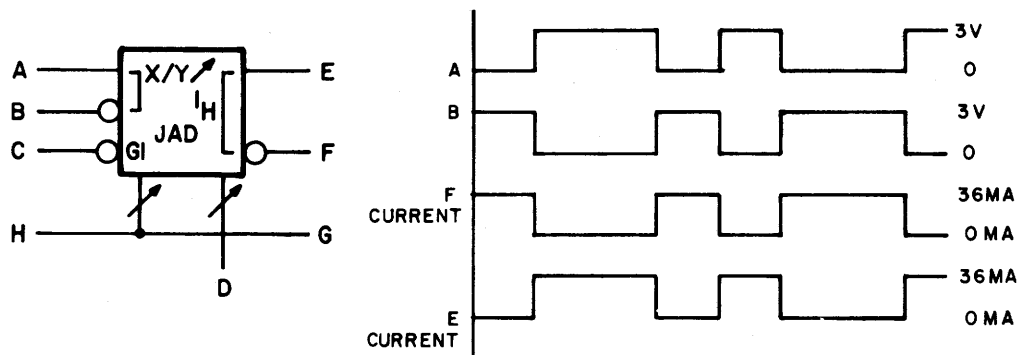
The JAD circuit (Figure 7-23) provides the write current to the read/write heads during a write operation. Circuit outputs E and F are connected across a pair of series-connected, write coils. When input A is positive, current flows from output E to ground via one of the coils. When input B is positive, current flows from output F to ground through the other coil.

When a positive signal is present at input A, QN turns on dropping the collector of QN to near zero volts. This causes QP to turn off and no current flows at output F. At this same time QR is off since input B is at zero volts. Base drive is applied to QQ via resistors NR5 and NR3 and as a result is on. With QQ on, current flows from output E. (This current is limited by external resistors connected between E and F and their respective coil.) When the inputs are reversed (B positive and A at zero volts) the circuit conditions reverse, and current flows from F. Transistor QS, and related components, provide a constant current source for the emitters of QN and QP.

Input C functions as an inhibit to the circuit. Input C must be at a +40-volt level when a write operation is in progress. When a write operation is not occurring, C is at zero volts and the bypass action of diodes NCR1 and NCR2 prevents base drive to both QP and QQ. This action stops current flow from both outputs E and F.

The level of current used during a write operation is selected by external circuits in accordance with the track location of the heads. If the actuator has positioned the heads to a track between, and including, 0 and 127, write current (at input H) is derived from +40 volts. If the heads are at track 128 or above, input H is at +35 volts and the available write current is reduced.

Output G provides write current to an external current monitor circuit.

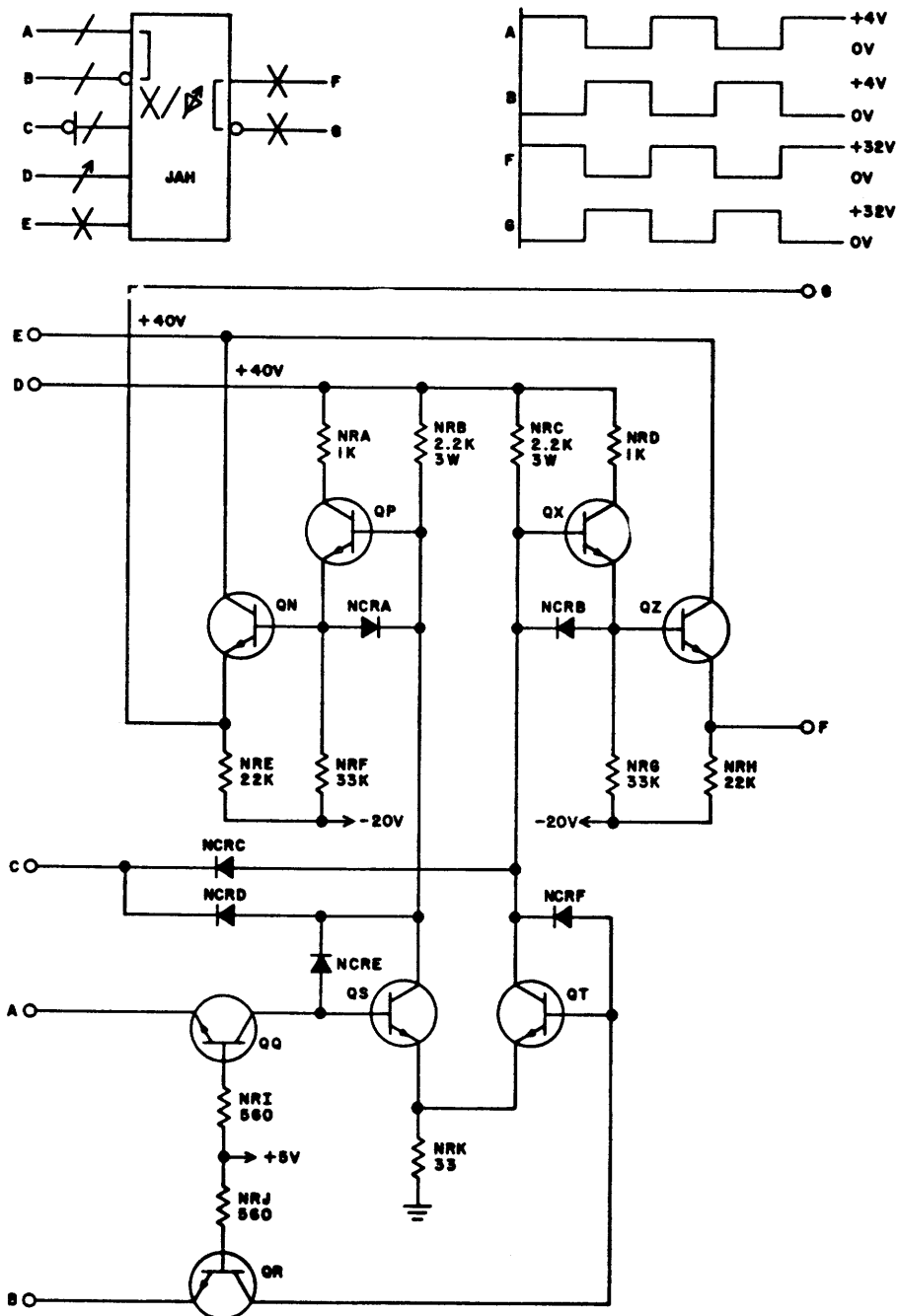


NOTE:

I. VOLTAGE AND COMPONENT VALUES FOR REFERENCE ONLY

6T152

Figure 7-23. Write Driver - JAD



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7K35

Figure 7.23.1. Write Driver - JAH

Write Driver - JAH

The JAH circuit is a symmetrical driver that amplifies the write signal for recording on the disk. Points A and B are inputs to the driver. Points F and G are outputs. Point C is the write gate input. Points D and E go to +40 vdc switched through an external resistor.

Transistors QQ and QR connect to a toggle FF as an interface to the driver transistor QS and QT. With the input at A high (+4 vdc), QQ is reverse biased, base to emitter. Current flows from base to collector and turns on QS. At the same time, input B is low (ground) which turns QR on. This puts a ground at the base of QT, holding it off.

Transistors QN and QP are a darlington pair with the drive for QN coming from QP. When QS is on, QN is off because the base of QP is pulled to ground by QS. QZ, QX, and QT work in the same manner.

Diodes NCRA and NCRB speed up the turn off of QN and QZ by removing the base-emitter charge.

Diodes NCRC and NCRD are gating diodes that put a clamp to ground at the base of QP and QX when a ground is placed at point C.

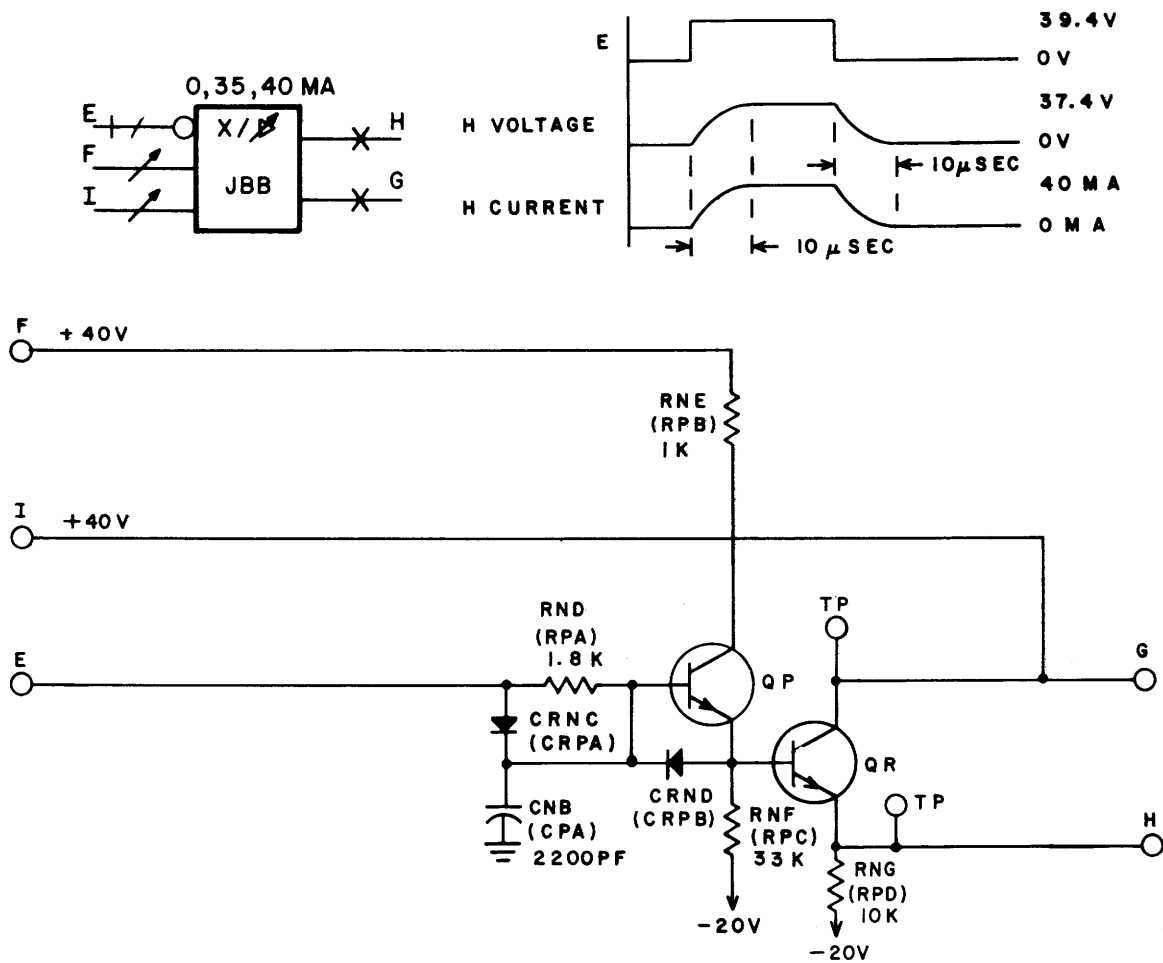
Diodes NCRE and NCRF are antisaturation diodes that keep transistors QS and QT from saturation.

Erase Driver - JBB

The JBB circuit controls the current driving the erase heads. When input E (Figure 7-24) is a high voltage, output H provides current to erase heads.

When input E goes to a high voltage, capacitor CPA charges, causing a 10-usec delay before transistors QR and QP turn on completely. Output G is connected to a +40v supply in a fault detect circuit. When QR is on, current flows from G through QR to the erase head connected to output H. The ramp output protects the information on neighboring tracks from being destroyed.

When E drops to 0v, CPA discharges through RPA. After 10 usec, QP and QR are off. Output H is at 0v.



NOTES:

1. VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

6T107

Figure 7-24. Erase Driver - JBB

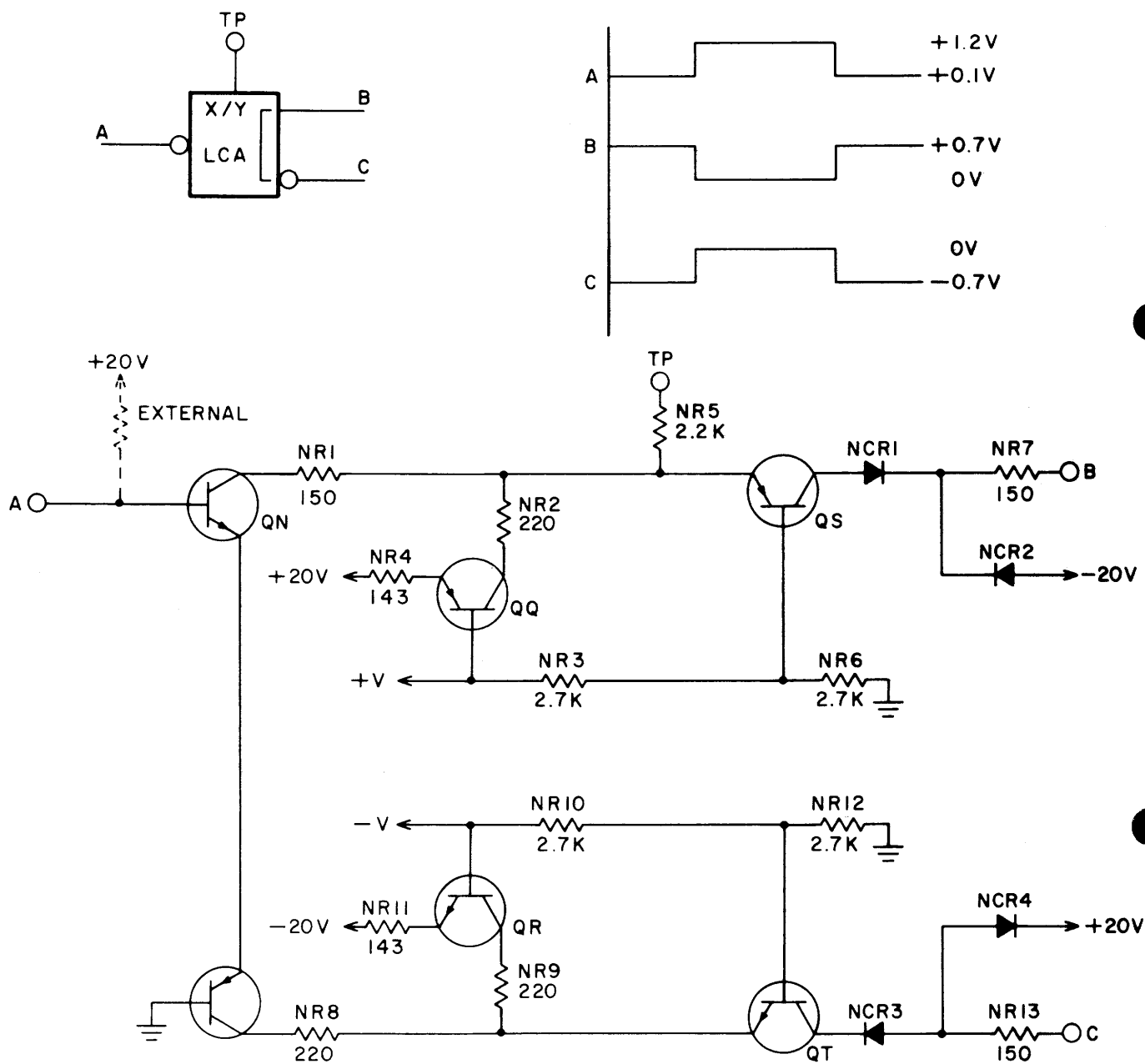
Line Transmitter - LCA

The LCA circuit (Figure 7-25) provides a positive output at B and a negative output at C when input A is low. When the input is high, outputs B and C are at ground.

The circuit is (and must be) driven with an open collector integrated circuit. The LCA circuit input is a differential stage (QN and QP) which sinks the current from the minus and plus constant current sources (QQ and QR) whenever input A is high. When A is high, QN and QP are off and the 25 ma of current from the constant current sources is routed through the emitters of the differential output stages (QS and QT) to the outputs B and C. External Zener diodes on the plus and minus voltage supply lines serve as a common voltage divider for all circuits on one card and provide bias voltage to the constant current sources and the output transistors.

The complementary current sink (QN and QP) monitor a close phase relationship during turn-on and turn-off by having the emitter of QN (NPN) drive the emitter of QP (PNP). Returning the external resistor on the circuit input to +20 volts, instead of +5 volts, ensures that QN and QP will sink the drive current if the +5-volt power is lost.

NCR2, NCR4, NR7, and NR13 protect the transmitter if large externally produced transients should appear on the output lines.



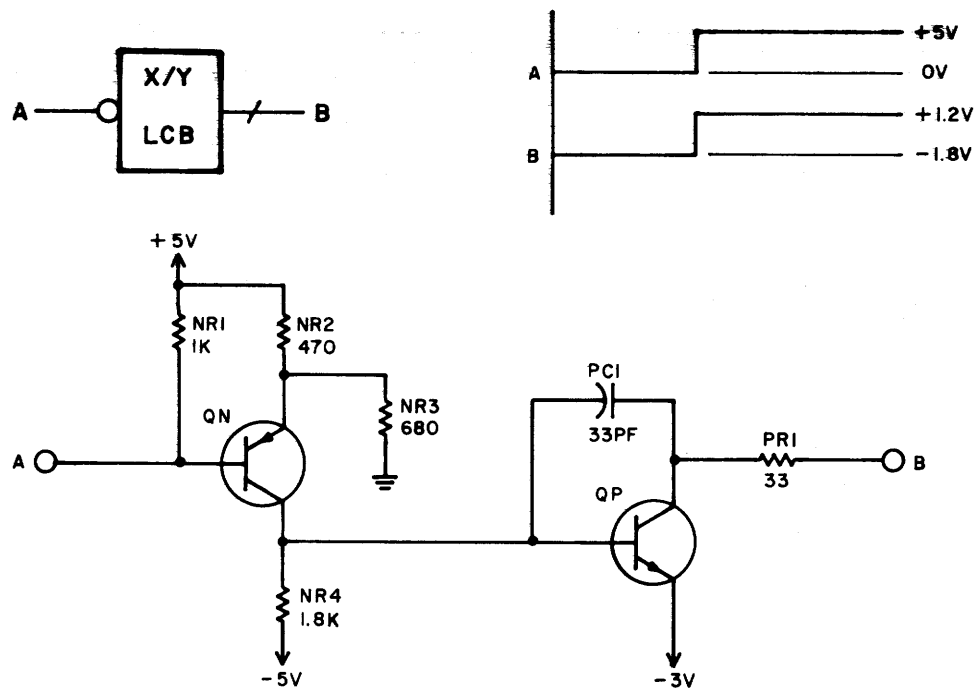
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

6T147

Figure 7-25. Line Transmitter - LCA

Line Transmitter - LCB

The LCB circuit (Figure 7-26) is a Q-level party-line transmitter that sinks current from the output line, B, to -3 volts when input A is at zero volts. When A is positive, transistor QN is reverse biased and both QN and QP are off. Capacitor PC1 controls the output rise and fall times.



NOTE :

1. VOLTAGE AND COMPONENT VALUES FOR REFERENCE ONLY

6T153

Figure 7-26. Line Transmitter - LCB

Oscillator - MAC

The MAC circuit (Figure 7-27) produces an amplified, oscillating signal at a prescribed frequency. The circuit description is divided into three parts: the D.C. conditions throughout the circuit; the oscillator section of the circuit; and the amplifier circuit.

D.C. Conditions

CRNA, RNA, RNB and RND hold the base of QN at approximately +17 volts. CRNB is reverse biased by 3 volts and does not conduct. The emitter of QN is held at about +16v, producing a collector current in QN of about 16 ma.

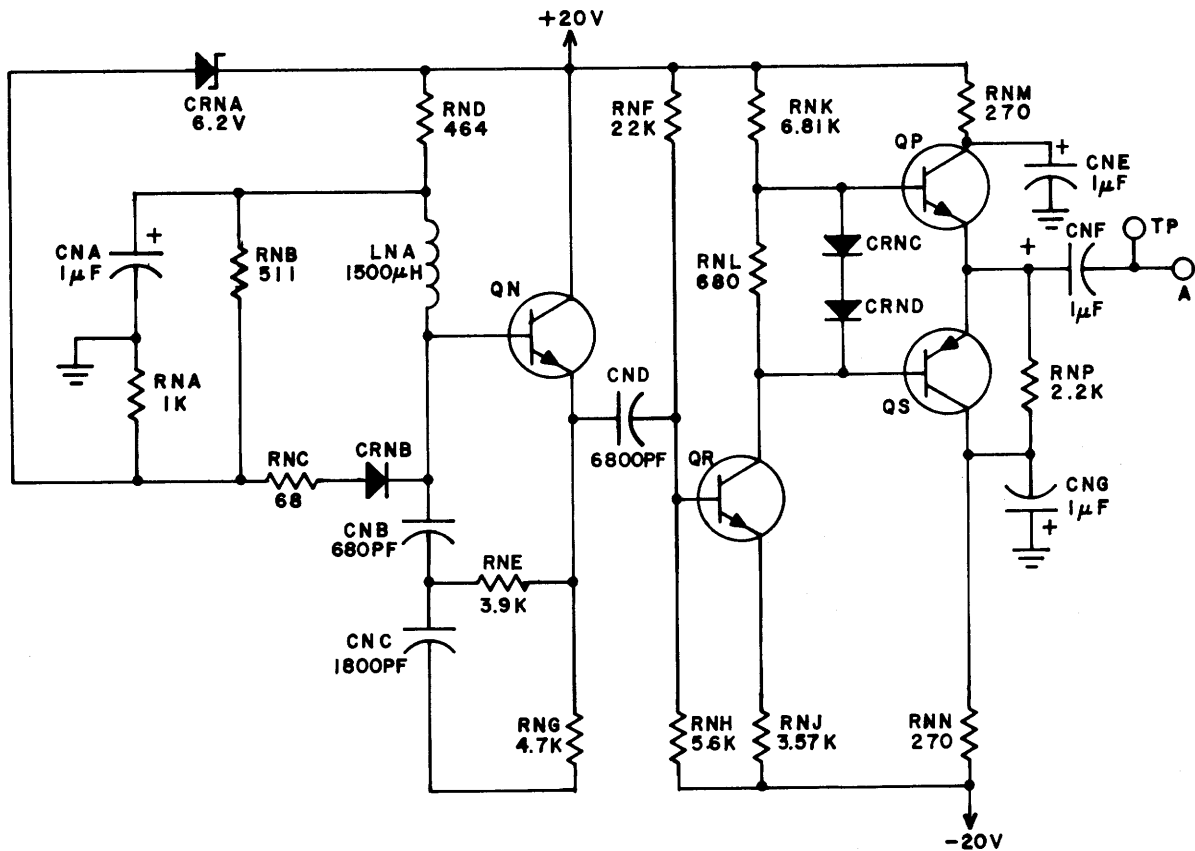
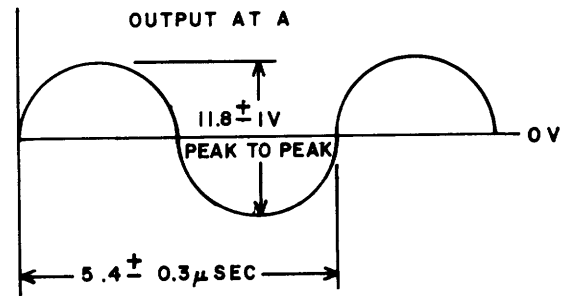
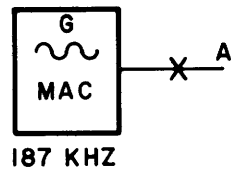
The base-emitter voltage drop across QR holds the base of QR near +0.7v. The current through RNH is then 5.1 ma. With the base current of QR at a low level, the 5.1 ma must flow through RNJ. The voltage at the junction of the emitters of QP and QS must then be about +10v. To maintain this +10v, the collector voltage of QR must be near +10v. The collector current of QR is, therefore, 5.55 ma.

Oscillator

Transistor QN acts as an emitter follower yielding a high current gain with nearly no voltage loss. CNB, CNC, and LNA form a resonant network. Near the resonant frequency, the signal voltage at the junction of LNA and CNB can be much greater than the voltage through RNE in the feed-back portion of the circuit. The gain around the loop formed by QN, RNE, CNB and LNA is greater than 1. The system, therefore, oscillates. When the signal at the base of QN exceeds 6v peak to peak, QN approaches saturation, thereby limiting the amplitude of the oscillation.

Amplifier

Transistor QR is the basic amplifier providing a voltage gain of about 2. Diodes CRNC and CRND keep QP biased in its active region while keeping QS biased slightly on. QP and QS are emitter followers that provide a low impedance output. As the voltage at the base of QP increases, the output voltage increases and charges the output capacitance. RNP is essentially the emitter follower resistance. As the base voltage decreases, QS turns on harder and provides a low impedance path to ground to discharge the capacitance and thereby provide an undistorted sine wave output. Capacitors CND and CNF provide dc isolation, and CNE and CNG are bypass capacitors.



NOTE:
VOLTAGE AND COMPONENT
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6T108

Figure 7-27. Oscillator - MAC

Oscillator - MAD

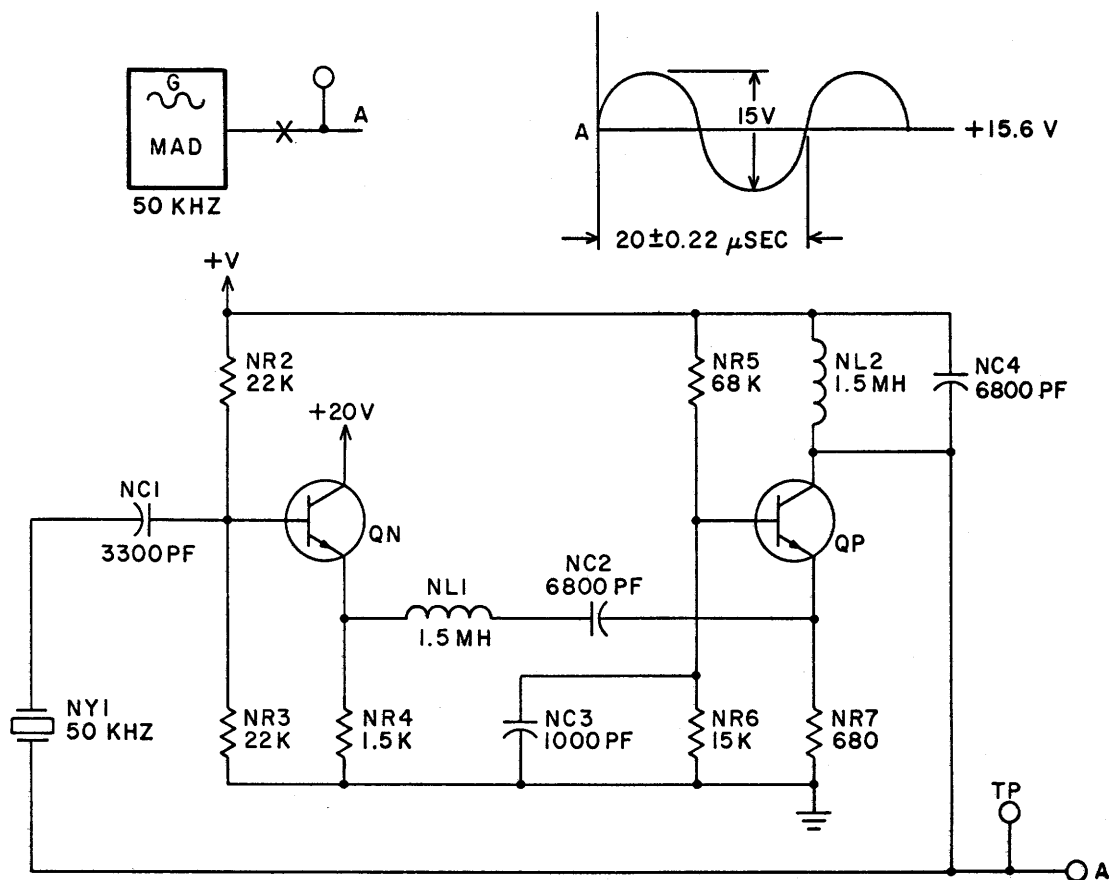
The MAD circuit (Figure 7-28) consists of a tuned voltage amplifier stage, QP, and a series tuned regenerative feedback path. The regenerative feedback path consists of a series tuned 50 kHz crystal, an impedance transformer (QN as an emitter follower), and a series LC pass network (NC4 and NC2). The nominal output amplitude is 15 volts peak-to-peak.

Oscillator - MAG

The MAG circuit (Figure 7-28.1) is a 50 kHz sine wave oscillator capable of supplying a 20V p.p. signal to point A.

The circuit is composed of three main functional blocks. Amp 1 is a narrow pass band filter operating at 50 kHz. Amp 2 is a gain of 0.89 inverting amplifier. Transistor QN and its associated circuitry is a level controlling AGC circuit.

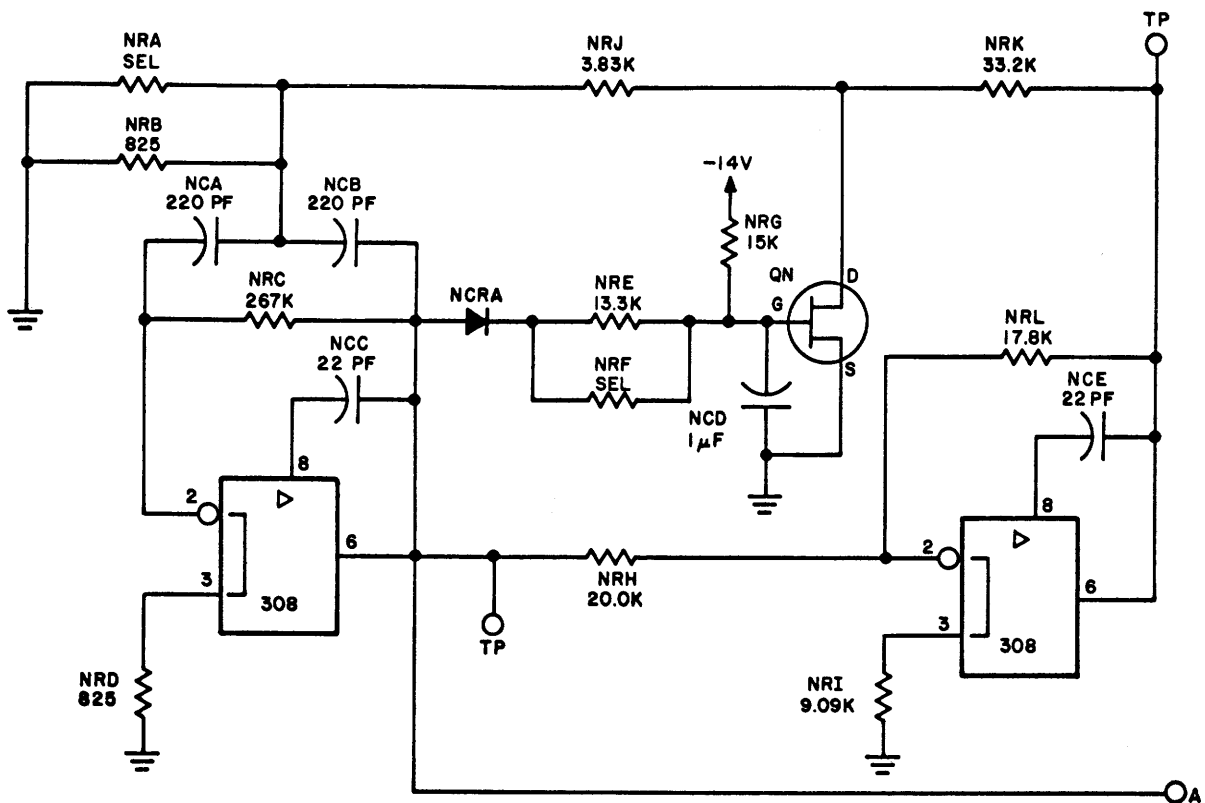
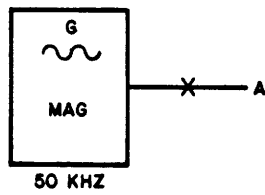
360° of phase shift on the oscillator circuit is accomplished by 180° on the bandpass filter and 180° on the Amp 2.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

6T138

Figure 7-28. Oscillator - MAD



NOTE: VOLTAGE AND COMPONENT VALUES FOR REFERENCE ONLY.

7K39

Figure 7-28.1. Oscillator - MAG

Ringin Amplifier - MBC

The MBC circuit (Figure 7-29) is a tuned amplifier which is rung by the negative clock and data pulses present at input A.

The tank circuit connected to the collector of QN is tuned (and is adjustable) to twice the frequency of the input data pulses (each data pulse falls between two clock pulses; absence of a data pulse is interpreted as a zero). The high Q of the circuit affords a flywheel effect and yields a sinusoidal signal that is almost totally free of peak shift.

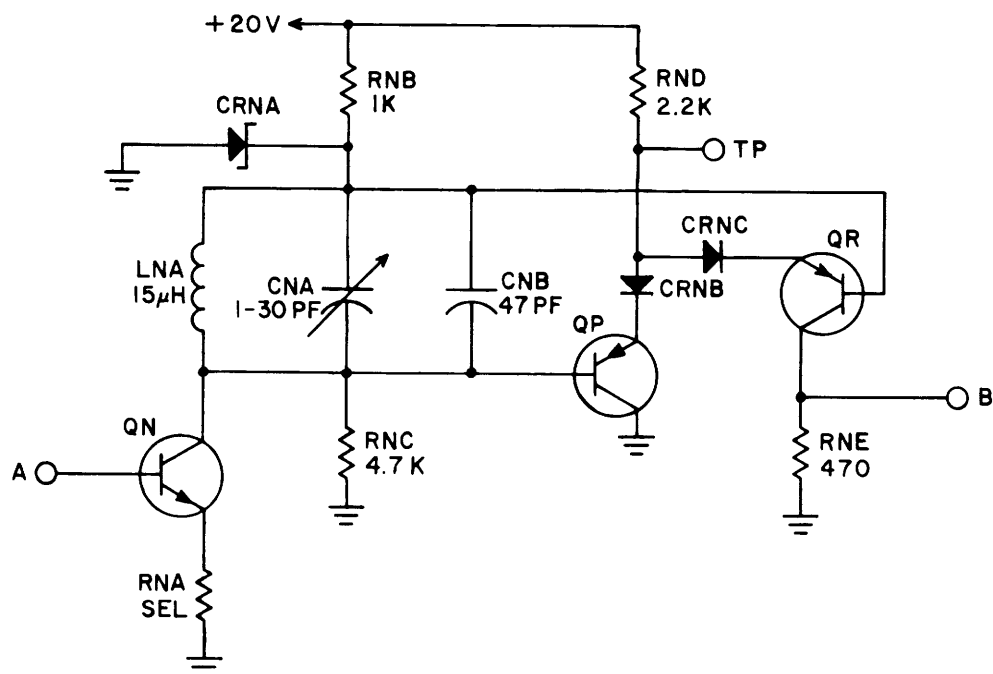
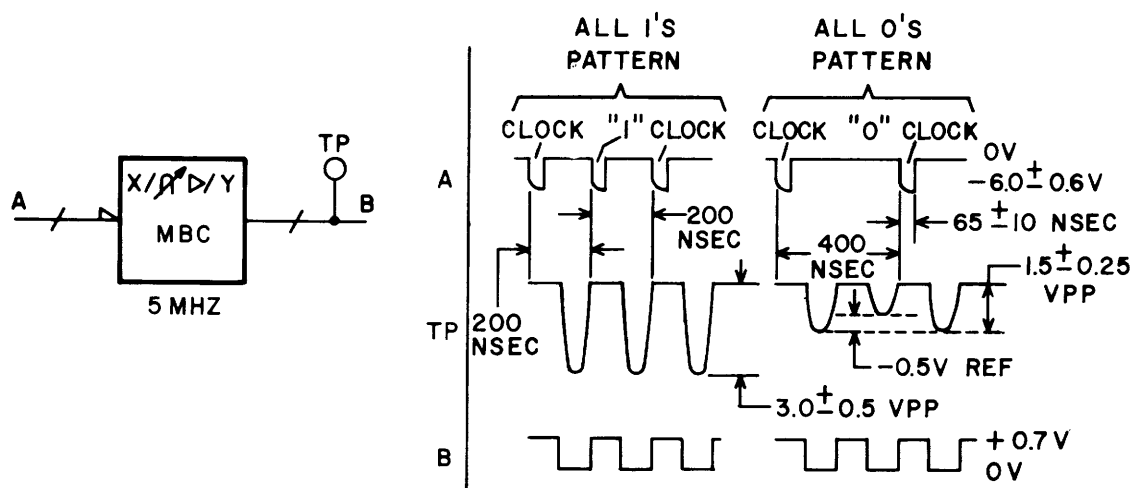
Transistors QP and QR form a zero-crossing detector, emitter follower circuit that provides high impedance so as not to distort the sine wave. The circuit clips the positive half of each sinusoidal excursion so that the signal at the TP is a half-wave rectified sine wave.

The transistor in the output load (next circuit) functions to clamp this rectified signal and to provide what is nearly a square wave output at B.

Quantizing Detector - QCA

Inputs A and B of the QCA circuit (Figure 7-30) are connected to the outputs of a sector transducer preamplifier. Each time a sector is detected by the transducer, a 55- μ sec "1" (+3v) pulse appears at output C. The input at A and B is an analog signal. The output at C is a standard logic signal.

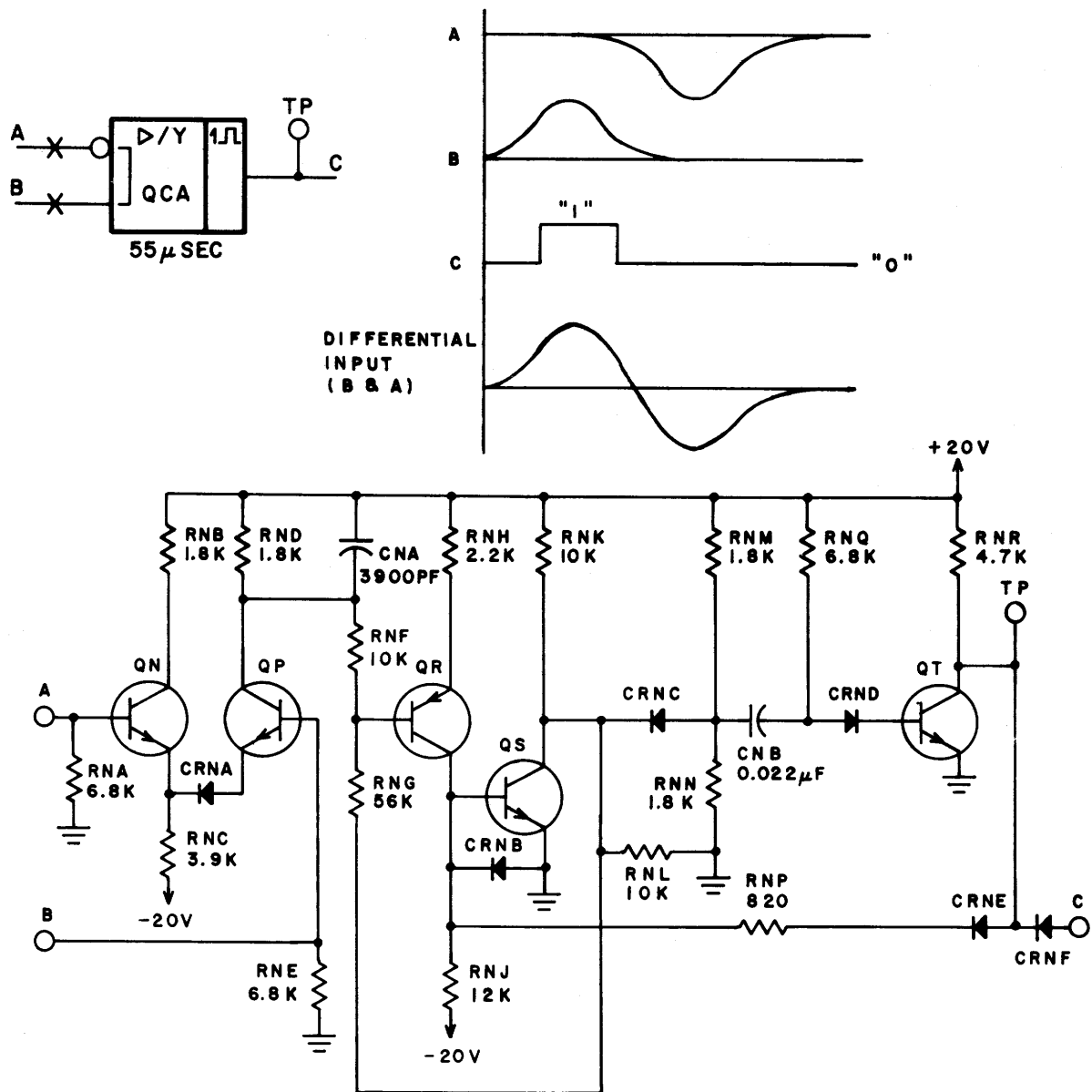
With a 0-volt differential input across A and B, diode CRNA holds transistor QP off, while transistor QN is on. The collector of QP is at about +19v. Transistor QR is, therefore, off. The base-emitter junction of QS is reversed biased through resistor RNJ. Transistor QS is off. Transistor QT is turned on by the forward bias supplied through resistor RNQ and diode CRND. With QT on, diode CRNF is forward biased and conducts current from output C through QT to ground. The output is near ground, or a "0".



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

8T109

Figure 7-29. Ringing Amplifier - MBC



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

6T110

Figure 7-30. Quantizing Detector - QCA

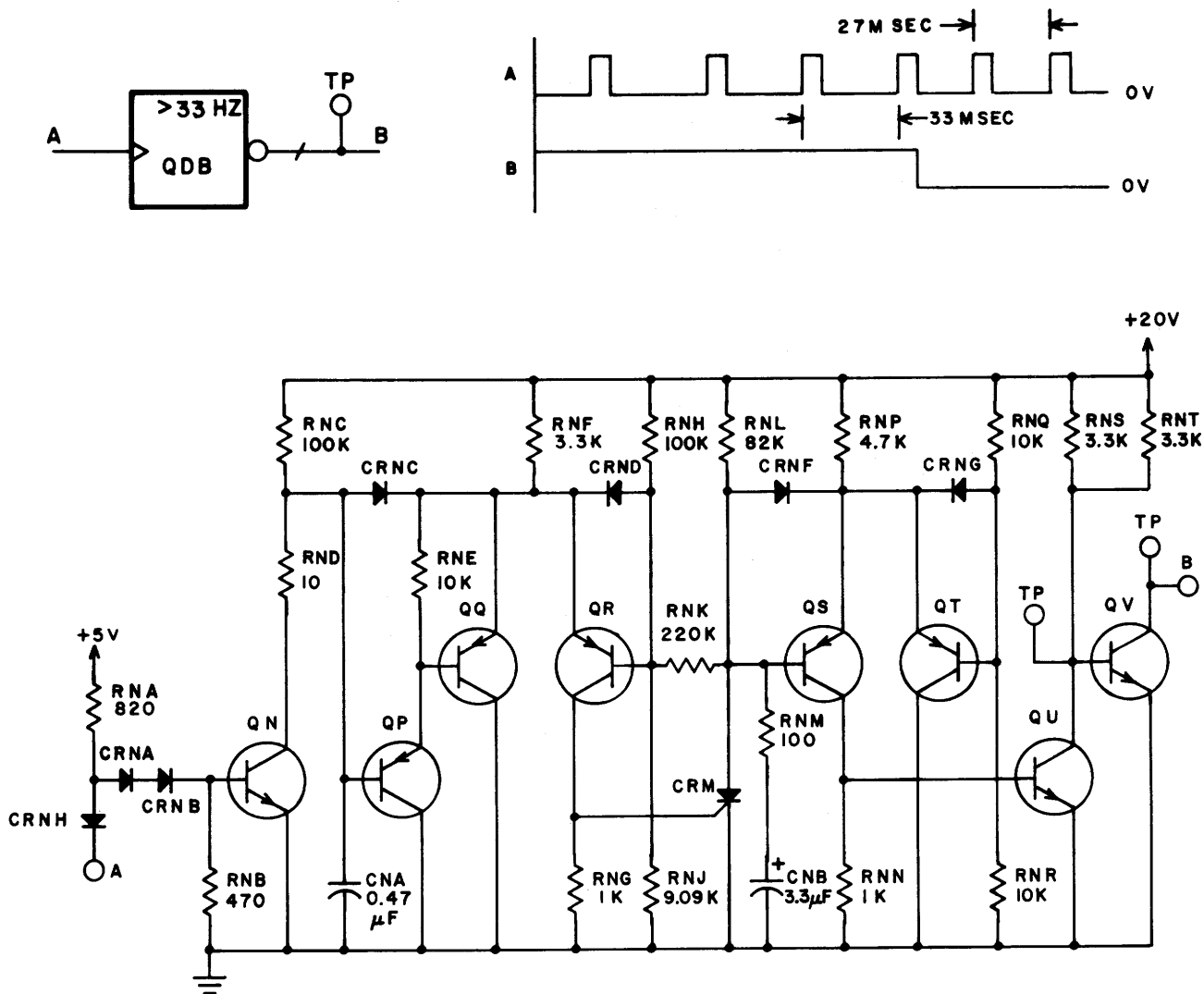
When a sector mark appears, the differential voltage across inputs A and B rises with B more positive than A. Transistor QP turns on and its collector voltage falls to about +11v. The drop in voltage is felt at the base of QR. Transistor QR turns on, raising the voltage on the base of QS. Transistor QS turns on. Transistors QS and QT comprise a single shot circuit whose pulse width is determined by resistor RNQ and capacitor CNB. Transistor QT turns off, reverse biasing diode CRNF. Output C rises to a "1" level. After 55 μ sec, CNB charges sufficiently to turn on transistor QT. Diode CRNF is again forward biased and the output returns to a "0". Resistor RNP provides feedback to keep QS on while QT is off.

Speed Detector - QDB

The QDB circuit (Figure 7-31) monitors sector pulses to determine whether the spindle is at a predetermined speed. If the spindle is below speed, no output is present. When the spindle reaches the desired speed (pulse rate of more than about 33 hertz), an output current activates the speed relay which signals the controller that the unit is up to speed.

Each time a sector is sensed, a short "1" pulse is applied at input A. Transistor QN conducts and completely discharges capacitor CNA through RND to ground. When the pulse is removed, CNA charges through RNC. When the base of QP reaches the voltage at the base of QR, QP and QQ turn off. Transistor QR conducts current to silicon controlled rectifier CRM, turning it on. CRM draws current from the base of QS driving it to ground, and from the base of QR through RNK. The base of QR falls to about 9.03 volts. QR then turns on firmly and prevents "runt spikes" on the signal to CRM. Once CRM is turned on, CNB begins discharging through RNM and CRM. CRM remains on until the discharge current from CNB falls below the holding current of CRM (typically 1 ma). With the base of QS near ground, QS conducts. Transistor QT turns off, QU is on, and QV is off. No output signal is felt at B.

If the spindle is below speed, pulses arrive at the input at a low repetition rate. CNA repeatedly discharges and recharges to the point where QP and QQ are turned off. The output of QR is a series of positive pulses with a pulse width determined by $T = T_1 - T_C$ where T_1 is the time between input pulses and T_C is the time for CNA to change to the point where QP is turned off. The pulses repeatedly trigger CRM. CRM holds the voltage at the base of QS below the point where QS can turn off. Since QS is constantly on, QV is constantly off. No output is felt at B.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

6T146A

Figure 7-31. Speed Detector - QDB

When the spindle reaches the required speed, the pulses at input A have the same period as T_C . The pulse width out of QR becomes $T_1 - T_C = 0$. Transistor QR never emits a pulse. With no pulses out of QR, CRM never turns on. This permits CNB to charge to the point where QS is constantly off. The higher voltage at the base of QS is fed back to the base of QR through RNK to raise the voltage required across CNA to turn off QP. This feedback prevents rapid fluctuation of the output when the spindle is near the required speed. With QS constantly off, QU is off and QV is on. Current flowing through QV activates the speed relay connected to B, and signals the controller that the unit is up to speed.

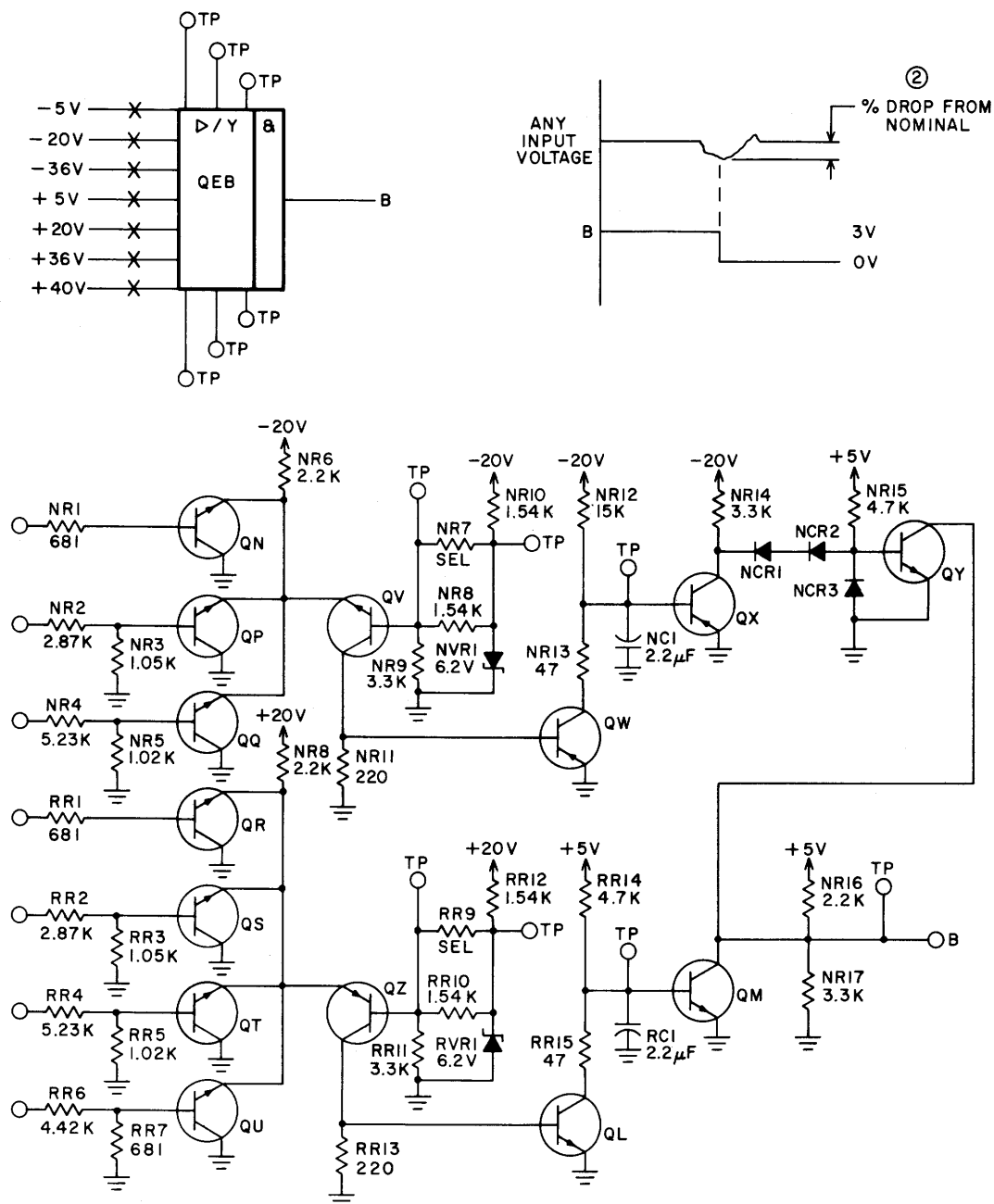
Voltage Checker - QEB

The QEB circuit (Figure 7-32) detects any decrease in voltage supply greater than a specified percentage. A fault condition will occur if:

1. -20 supply decreases below -18v
2. +20 supply decreases below +18v
3. +40v supply decreases below +36v
4. -36v supply decreases below -28.8v
5. +36v supply decreases below +28.8v
6. -5v supply decreases below -4.75v
7. +5v supply decreases below +4.75v

If all positive supplies are normal, QR, QS, QT and QU are off. Their emitters are held at +6.2v by Zener diode RVR1 and the value of RR9 (determined by testing to give a precise collector voltage). Current is pulled through QZ, causing a voltage drop across resistor RR13. This voltage drop turns QL on. Transistor QM turns off. If any of the voltage supplies drop below the specified percentage of their operating values, the respective transistor turns on. Transistor QZ will then be off. Transistor QL turns off. Transistor QM turns on, driving the output to ground.

The negative voltage segment of the circuit is similar to the positive section. A decrease in the -20v supply below -18v will turn QP on. Transistor QV turns off, causing QW to turn off. Transistor QX turns on causing a voltage drop across NR14 which turns QY on. The output drops to ground.



NOTES:

1. VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

② 5% DECREASE FROM NOMINAL $\pm 5V$, 10% DECREASE FROM NOMINAL $\pm 20V$ OR $\pm 40V$, OR 20% DECREASE FROM NOMINAL $\pm 36V$.

6T143

Figure 7-32. Voltage Checker - QEB

Quantizing Detector - QFA

The QFA circuit (Figure 7-33) detects a fault in the write and erase drivers or in the head select circuit. If there is an open in the head, either of the drivers is non-functional, or more than one head is selected, a fault signal occurs.

Inputs A and B are connected to the write and erase driver circuits and enter across a voltage bridge to the base of QP. Normally, both inputs are approximately 32v. All diodes are forward biased. Voltage on the base of QP is 32v and the emitter is at 31.4v due to a reverse bias 0.6v base-emitter voltage across QP. Transistor QP is off. All input current goes to ground through RND.

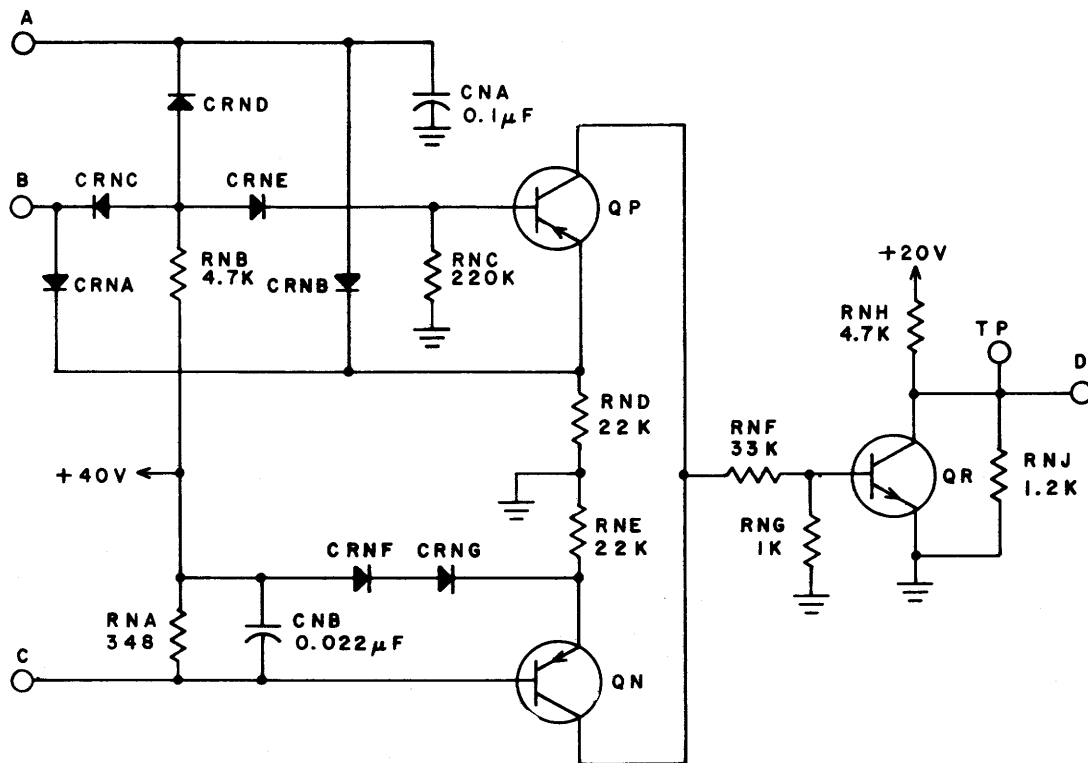
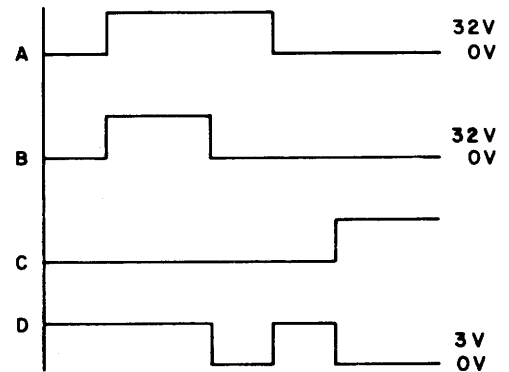
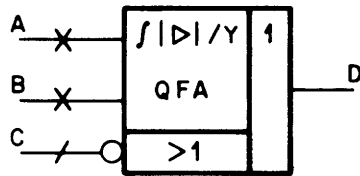
If input A is higher than input B by 1.4v, CRNB and CRNC are forward biased. CRNA and CRND are reverse biased. The voltage on the base of QP becomes that of input B. The emitter of QP is 0.7v higher than the base due to a 0.7v drop across CRNB. Transistor QP is on.

If input B is higher than input A by 1.4v, CRNA and CRND are forward biased. CRNB and CRNC are reverse biased. The base of QP is at the voltage of input A. The emitter of QP is 0.7v higher than the base. Transistor QP is on.

Input C is connected to the head select circuits. If more than one head is selected, the drop in effective resistance (due to external resistors in parallel) results in an increase in current through RNA. This increases the voltage drop across RNA, turning QN on.

If either QN or QP is on, QR turns on. Output D goes to ground to signify a fault condition.

FAULT =>1.4V DIFF OR >1 HEAD SEL



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

6T111

Figure 7-33. Quantizing Detector - QFA

Quantizing Detector - QFB

The QFB circuit (Figure 7-34) is used to amplify and shape an incoming wave. The input at A and B is a differential sine wave. The output at C and D is an amplified and clipped version of the input wave.

Transistor QR is the current source for the differential amplifier stage consisting of QN and QP. Capacitors CNA and CNB filter out dc and low frequency noise and pass the input wave which alternately turns on QN and QP. The output at the collectors of QN and QP are clipped by diodes CRNA and CRNB to approximate a square wave. This square wave is fed to the bases of QS and QT for another stage of differential amplification. The square wave output at the collectors of QS and QT is again clipped by diodes CRNC and CRND. The output at C and D is a clipped, square wave between 0v and +0.6v corresponding to the rise and fall of the sine wave at inputs A and B, respectively.

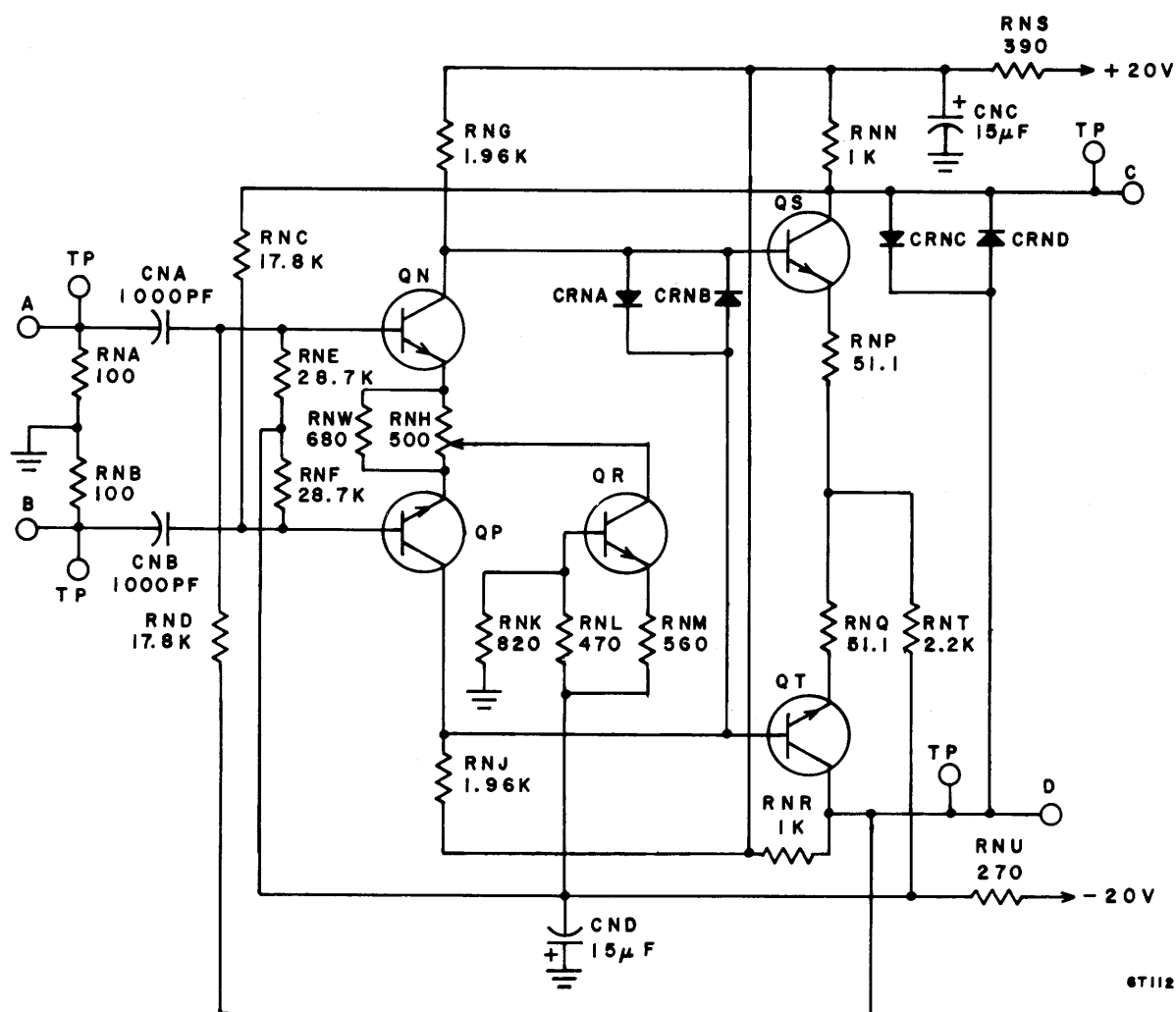
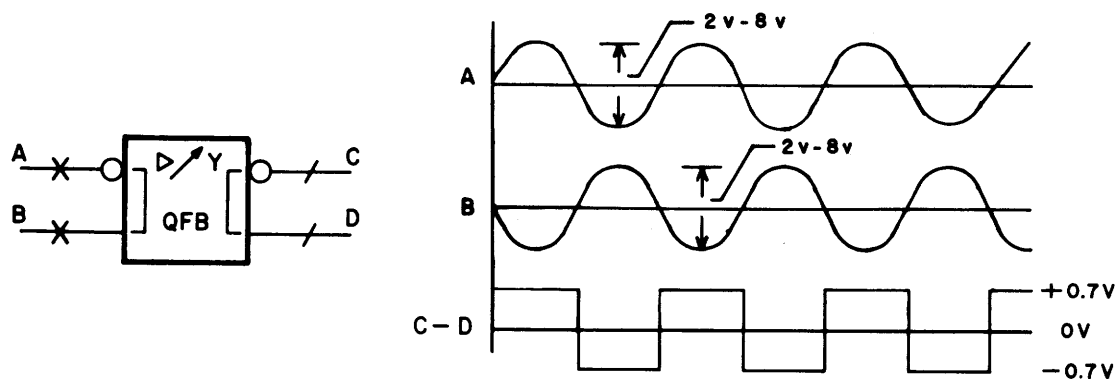
Single Shot - QFF

The QFF circuit (Figure 7-35) produces a positive pulse output in response to a positive input pulse. The width of the output pulse is independent of the input and is adjustable.

Assume a condition where QN is on. With the collector of QN at ground, QP turns off and CNC begins charging (through RNL to ground via QN and QS) toward vcc volts. The duration of the charging period is controlled by the time constant $RNL \times CNC$. When the base of QQ reaches 0.7 volts, QQ turns on, QS turns off, and the output goes to ground.

With the circuit in the condition of the preceding paragraph, a no-signal state will have the following effect: Ground level at base of QN turns it off. Since QS is also off, current is drawn through the base of QP and turns it on. Current now flows through QP charging CNC in the opposite direction (from preceding paragraph) to about -5.3 volts (Zener diode CRNC voltage minus the 0.7 base-emitter voltage of QQ). As the current increases and decreases (during charging period) through QP, the remaining current still flows through RNL thereby keeping QQ on.

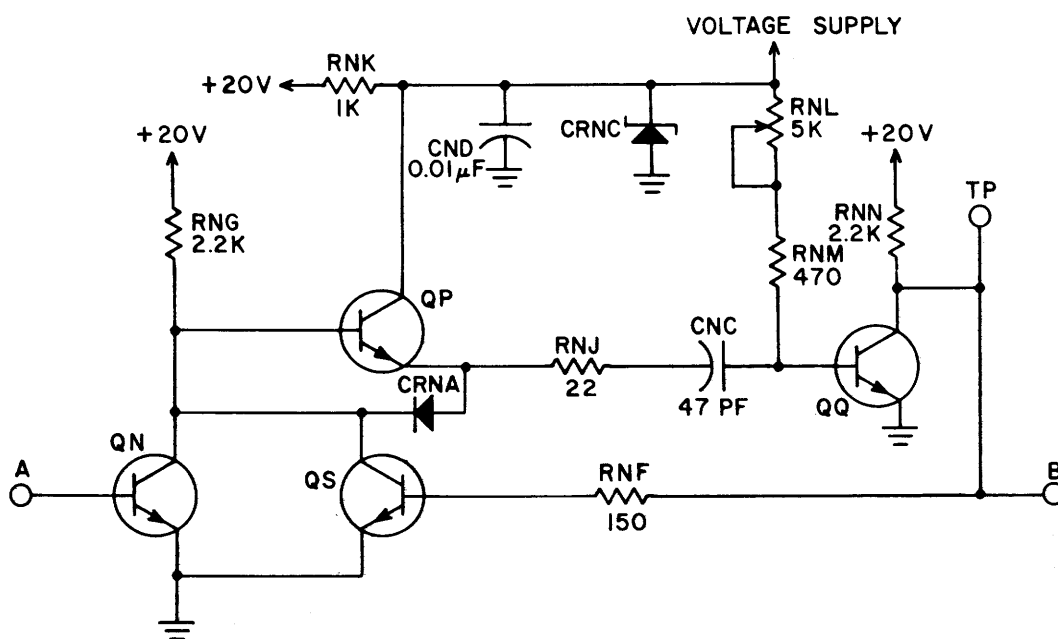
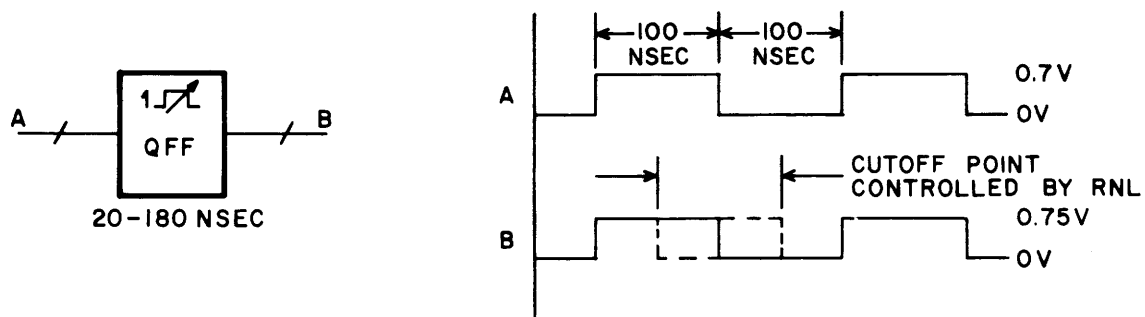
When a clock or data pulse is applied to the base of QN it turns on. With the QN collector at ground, QP turns off and a -5.3 base-emitter voltage appears across QQ. Capacitor CNC again charges through the variable resistor RNL until QQ turns on.



6T112

NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

Figure 7-34. Quantizing Detector - QFB



NOTE: VOLTAGE AND COMPONENT VALUES
ARE FOR REFERENCE ONLY.

8T113

Figure 7-35. Single Shot - QFF

When the circuit has been adjusted so that the width of the output pulse exceeds that of the input pulse, QS stays on (after the input drops) to hold the base of QP at ground.

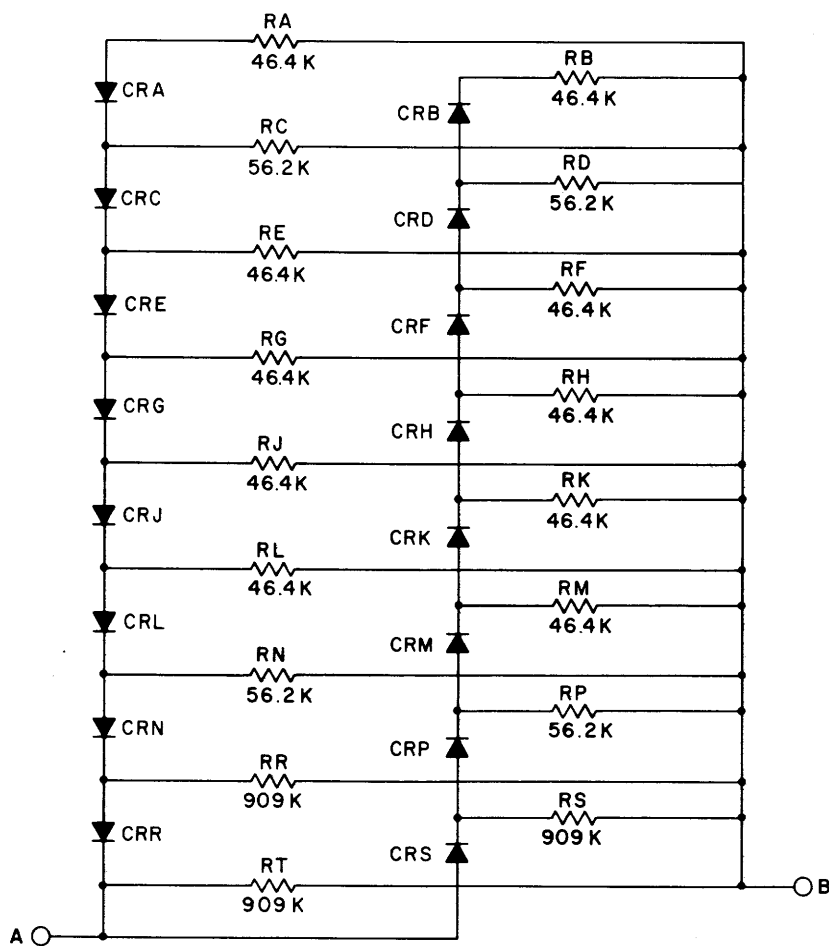
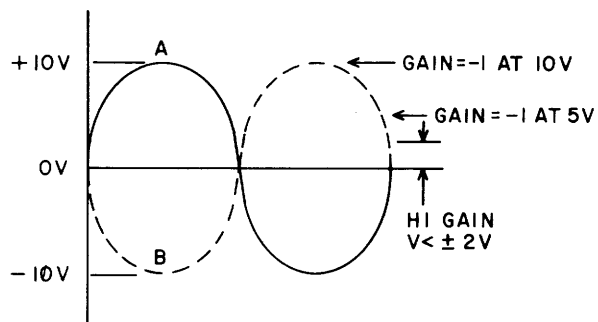
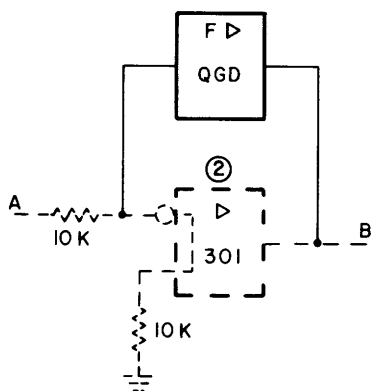
Whenever CNC is charging through RNL with current flowing through RNN, QN and QS are on to conduct the increase current.

Capacitor CND is a filter capacitor to provide a constant voltage across CRNC.

Function Generator - QGD

The QGD circuit (Figure 7-36) is a non linear feedback network used as the gain determining element for an operational amplifier.

With a 10K input resistor, an amplifier with the QGD circuit will exhibit high gain characteristics for amplifier output voltages of less than ± 2 volts. A gain of unity is achieved at output voltages ± 5 volts with this gain persisting at higher voltages.



NOTES: 1. VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.
 ② SHOWN FOR REFERENCE ONLY.

6T139

Figure 7-36. Function Generator - QGD

Line Receiver - RAB

The line receiver circuit, RAB, (Figure 7-37) provides a "1" output at C when the difference in input voltage (A minus B) is greater than +0.6v. Under any other input conditions, the output will be a "0".

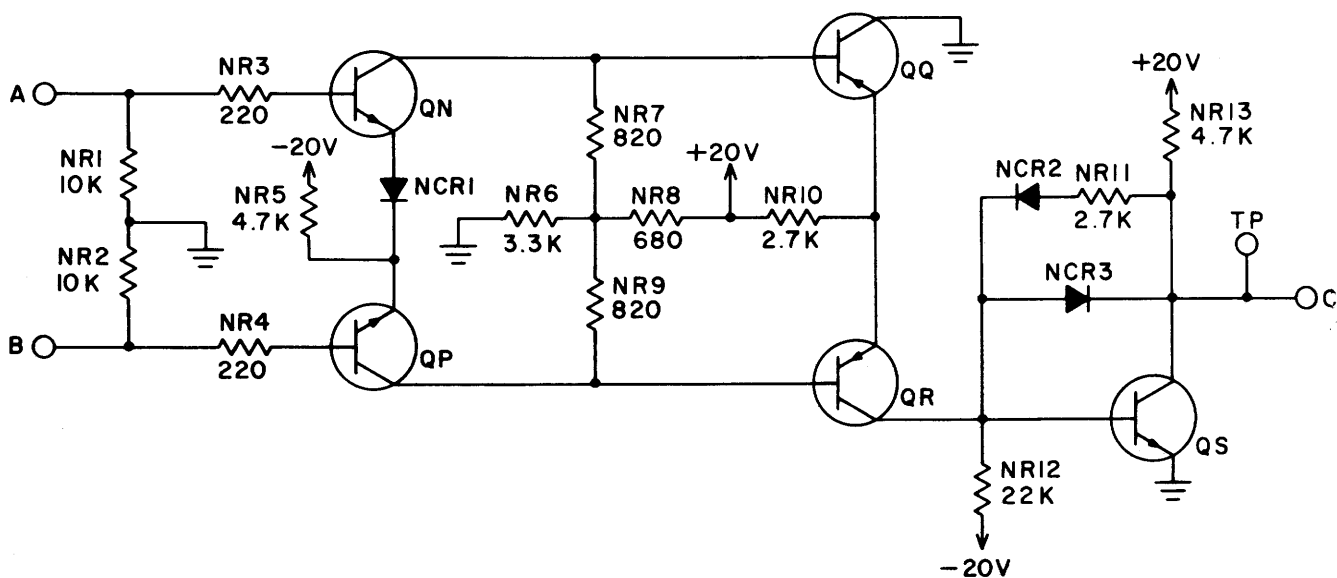
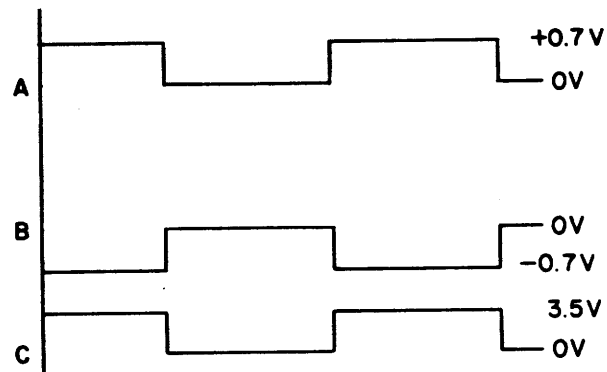
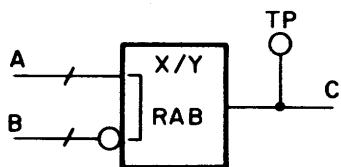
Diode NCR1 is used to maintain the threshold level at +0.6v. Without NCR1, the threshold would be about +0.1v. That is, if input B were just 0.1v less positive than input A, the circuit would switch to an output of "1".

Resistor NR5 supplies the emitters of QN and QP with a constant current of about 4.25 ma. If the current in one transistor increases, the current in the other transistor must decrease by an equal amount. If input B is more positive than input A (A minus B is negative), QP will be turned on and QN will be turned off. If the difference A minus B is only slightly negative, QP will conduct more than QN, but both will be on.

The base of QR, therefore, becomes more negative than the base of QQ. Transistor QR turns on, driving its collector and the base of QS positive. Transistor QS turns on, conducting current from the +20v supply through NR13 to ground. The output at C is near 0v or a "0".

If input A is at least +0.6v more positive than input B (A minus B is greater than or equal to +0.6v), QN turns on and QP turns off. The base of QQ is then more negative than the base of QR. Transistor QQ turns on, conducting current from the +20v supply, through NR10 to ground. Transistor QS is turned off as there is no current to its base. Current is then allowed to flow from the +20v supply, through the load resistors to output C. The value of the output voltage is approximately +3.5 volts or a "1".





NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

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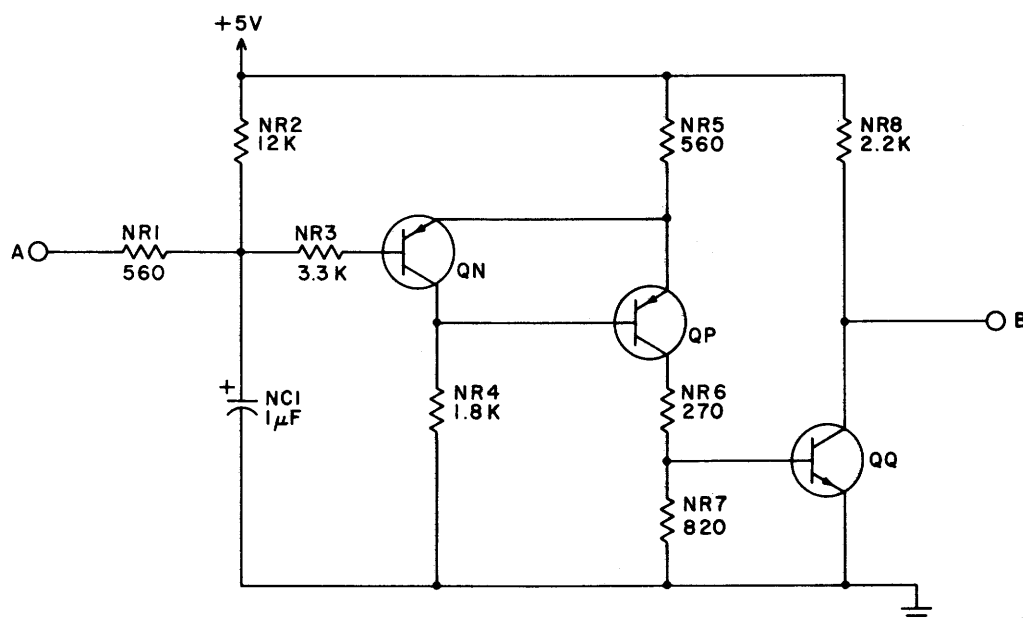
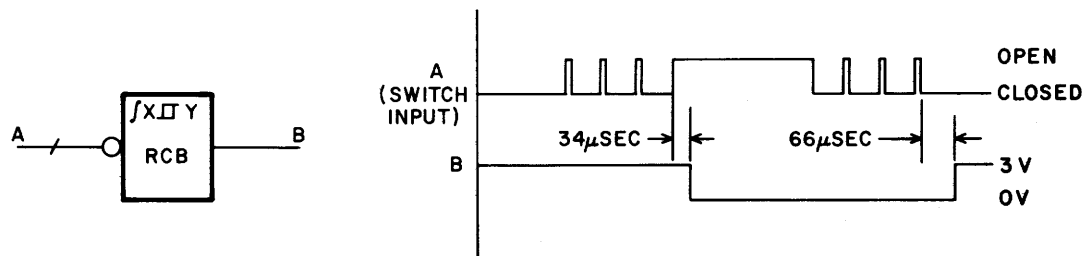
Figure 7-37. Line Receiver - RAB

Switch Receiver - RCB

Switch Receiver RCB (Figure 7-38) produces a "1" (+3v) output at B when the grounded switch connected to input A is closed. When the switch is open a "0" (0v) is felt at output B.

A switch to ground is connected to input A. When this switch is open, capacitor NC1 approaches +5v and QN is shut off. Transistor QP is, therefore, on and conducts current to the base of QQ through resistor NR6. Transistor QQ turns on, conducting current away from output B, and drops the output to near ground or a "0".

When the switch is closed, the voltage across NC1 rapidly increases through NR1 and the switch to ground because of the short time constant of NR1 and NC1. Any contact bounce on the switch will increase the discharge time. As the voltage across NC1 decreases, QN begins to turn on. As QN conducts current to the base of QP, the forward bias on QP is decreased and QP begins to turn off. As QP turns off, the current through NR5 decreases due to the higher lead resistance (NR4) of QN compared with QP (NR6). The current drop through NR5 causes a decrease in the voltage drop across NR5. The bias on QN is, therefore, increased. The cycle goes rapidly to completion. Transistor QP is shut off. With QP off, the base of QQ is near ground, causing QQ to shut off. This allows the +5v supply to flow through NR8 to output B raising the output to +3v, "1".



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

8T145

Figure 7-38. Switch Receiver - RCB

When the switch is opened again, NC1 charges slowly to +5v due to the long time constant of NR2 and NC1. Any contact bounce on the switch will hold NC1 well below the switching level of QN until the bouncing ceases. As the voltage across NC1 increases, QN begins to turn off. Transistor QP begins to conduct current away from the emitter of QN. Transistor QP turns on rapidly because of this positive feedback. The output then returns to "0".

Line Receiver - RFA

The RFA circuit (Figure 7-39) provides a non-standard "0" output at C when input A is at least 0.6v more negative than input B. Diode CRNA holds the threshold at 0.6v. Under all other input conditions, the output will be a non-standard "1".

If the differential input (A-B) is greater than 0.6v, transistor QP turns on and QN turns off. This drives the base of transistor QR more positive than the base of QQ. Transistor QR conducts current from the -20v supply, through RNK to ground. The output at C is near 0v.

If the differential input (A-B) is less than 0.6v, QN turns on and QP turns off. The base of QQ goes more positive than the base of QR. Transistor QQ conducts and a negative voltage is felt at output C.

Since a "1" is defined in MDD logic as the most positive voltage, the 0v output in the first case is interpreted as a non-standard level "1". The negative voltage output in the second case is, therefore, a non-standard level "0".

The receiver is self-terminated with 56 ohms to ground on each line.

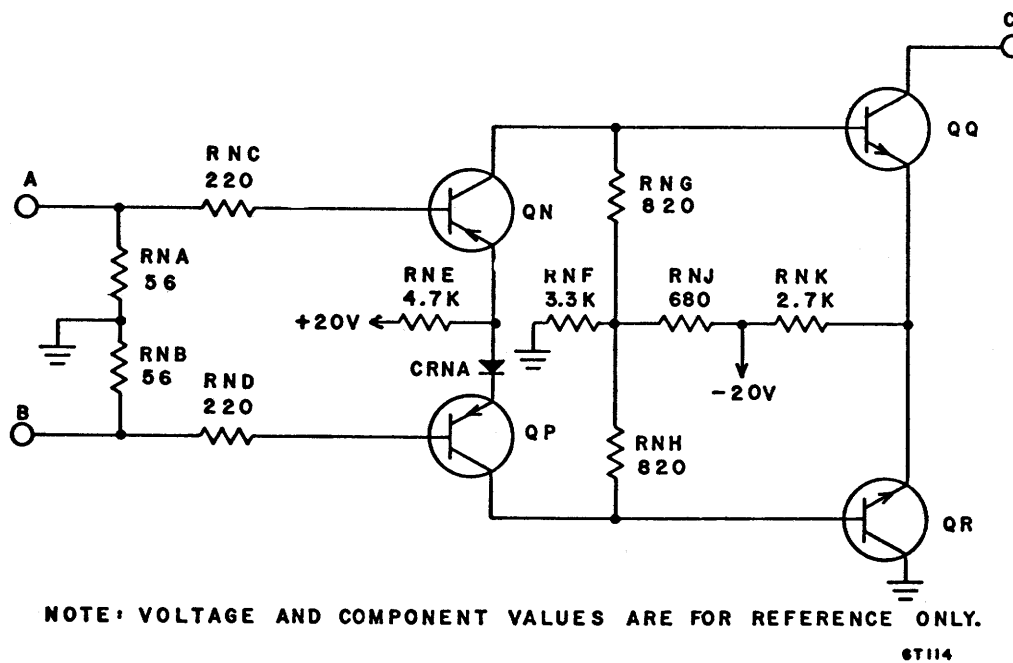
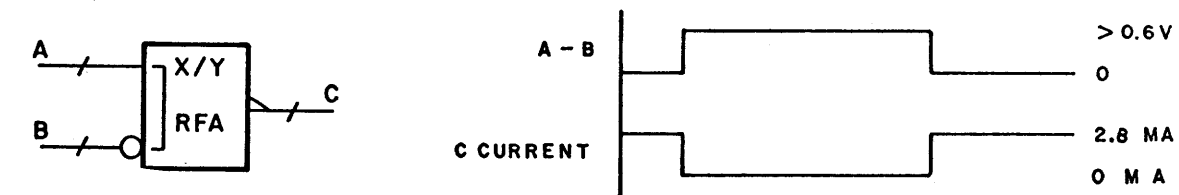
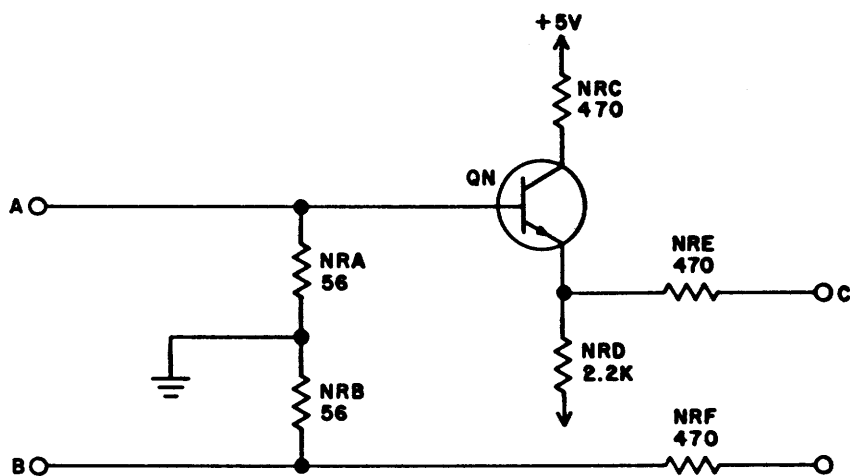
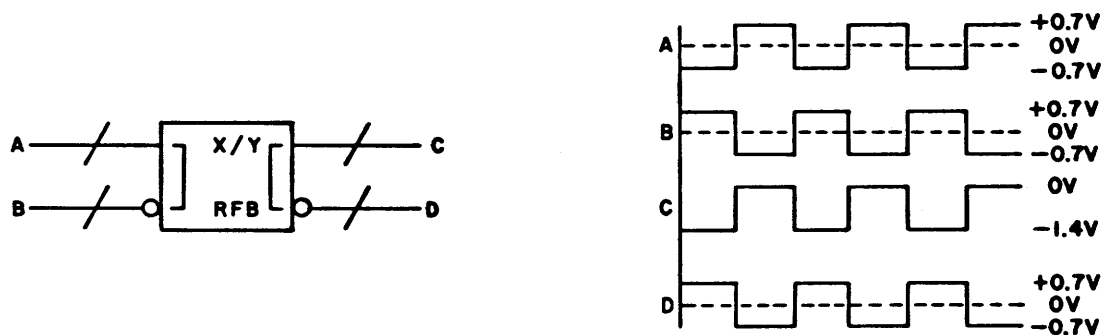


Figure 7-39. Line Receiver - RFA





NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7K29

Figure 7-39.1. Receiver Terminator and Offset - RFB

Receiver Terminator and Offset - RFB

Resistors NRA and NRB terminate write data from twisted pair inputs A and B. The same signal appears at input A and the emitter of QN except for the V_{BE} drop of 0.7v. This 0.7v maintains a differential voltage at outputs C and D, even when the I/O Line is open or non-operative. Outputs C and D feed into a receiver that switches each time the difference signal crosses 0 vdc.

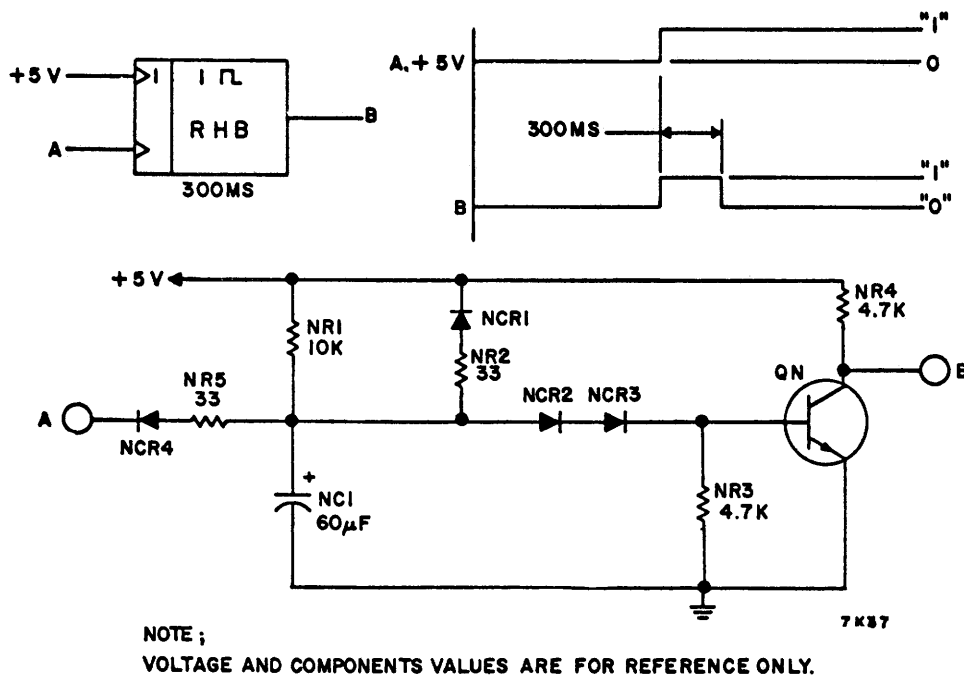


Figure 7-39. 1. Delay - RHB

Single Shot - RHB

The RHB circuit (Figure 7-39. 1) is a single shot that holds a clear signal on the units Fault register for 300 ms after +5 volts becomes available or the CLEAR FAULT switch on the logic chassis maintenance panel is pressed.

The circuit delay characteristic occurs as NC1 charges through NR1 to a threshold voltage of 2.1 vdc (determined by NCR2, NCR3, and base-emitter junction of QN). Register NR2 and diode NCR1 provide a quick discharge path for NC1 when the input drops. The presence of this path ensures a short recycle period for transient off/on application of the input.

Bipolar Current Buffer - SAA

The SAA circuit (Figure 7-40) is a power output stage for an operational amplifier. Transistors QP and QQ comprise a complementary output driver and are always biased slightly on by diodes NCR1 and NCR2.

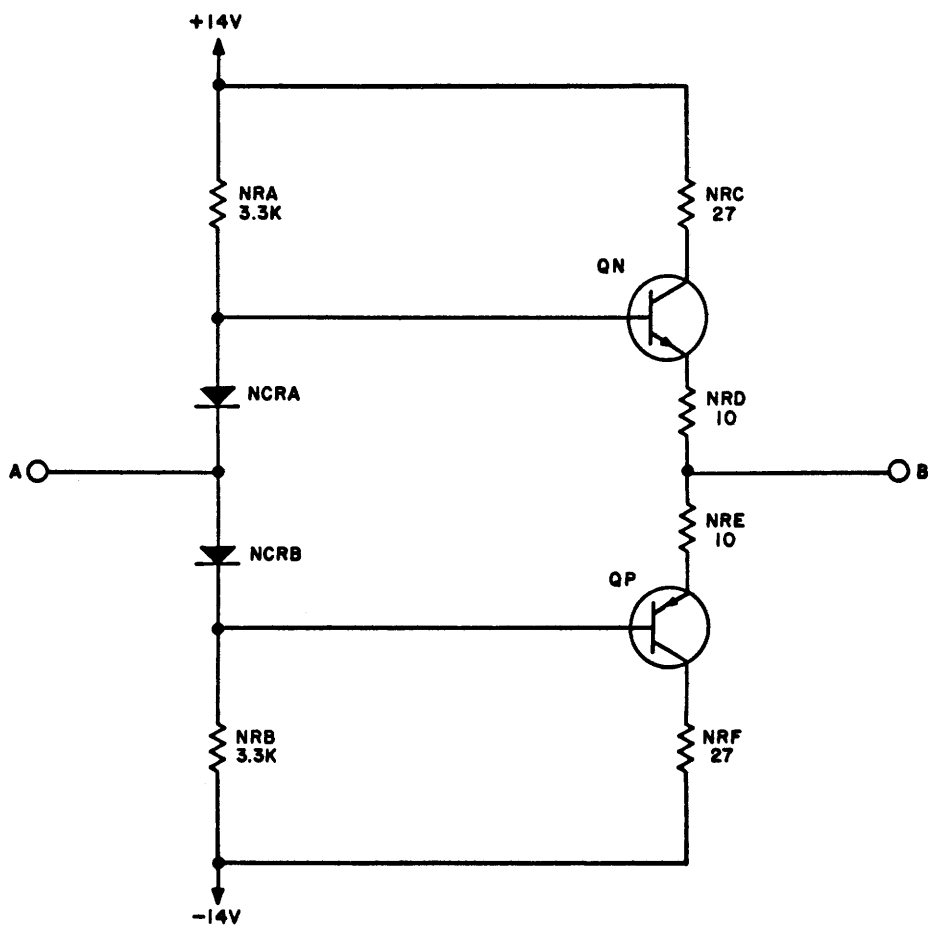
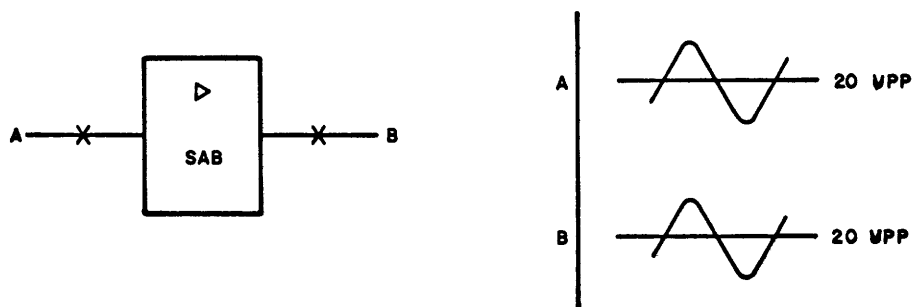
The quiescent current in the output driver is nominally 6.5 ma and the maximum signal amplitude for the circuit is ± 5 volts.

Amplifier - SAB

The SAB circuit (Figure 7-40.1) is a non-inverting, voltage gain of 1, current amplifier. The circuit provides high current drive capability for analog sources. (Like the MAG circuit.)

Fwd EOT Clamp - SAC

The SAC Circuit (Figure 7-40.2) is a TTL level operated current sink. The circuit sinks current from the position transducer demodulator circuit to prevent erroneous FWD EOT signals from appearing.



NOTE: VOLTAGE AND COMPONENT VALUES FOR REFERENCE ONLY.

7K40

Figure 7-40.1. Amplifier - SAB

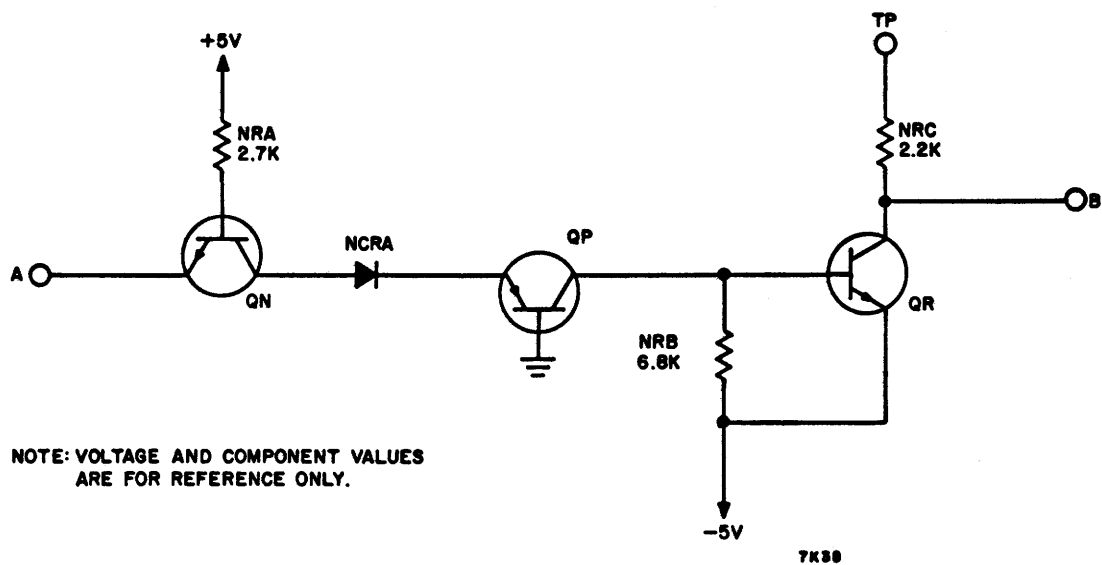
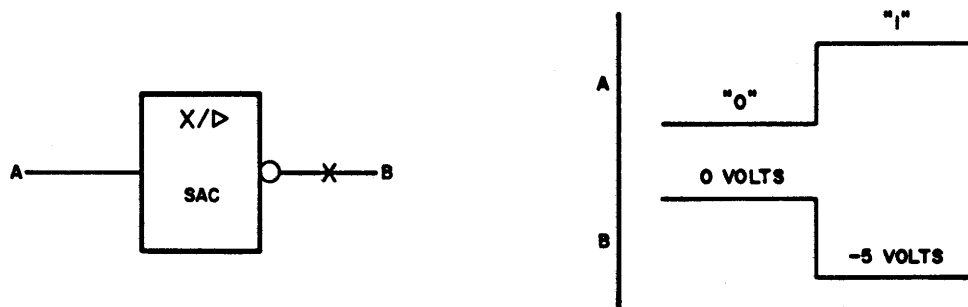


Figure 7-40.2. Fwd EOT Clamp - SAC

Demodulator - SBA

The SBA circuit (Figure 7-41) is a linear product detector operating on a fixed amplitude reference signal applied at input C and a variable amplitude information signal applied differentially across inputs A and B.

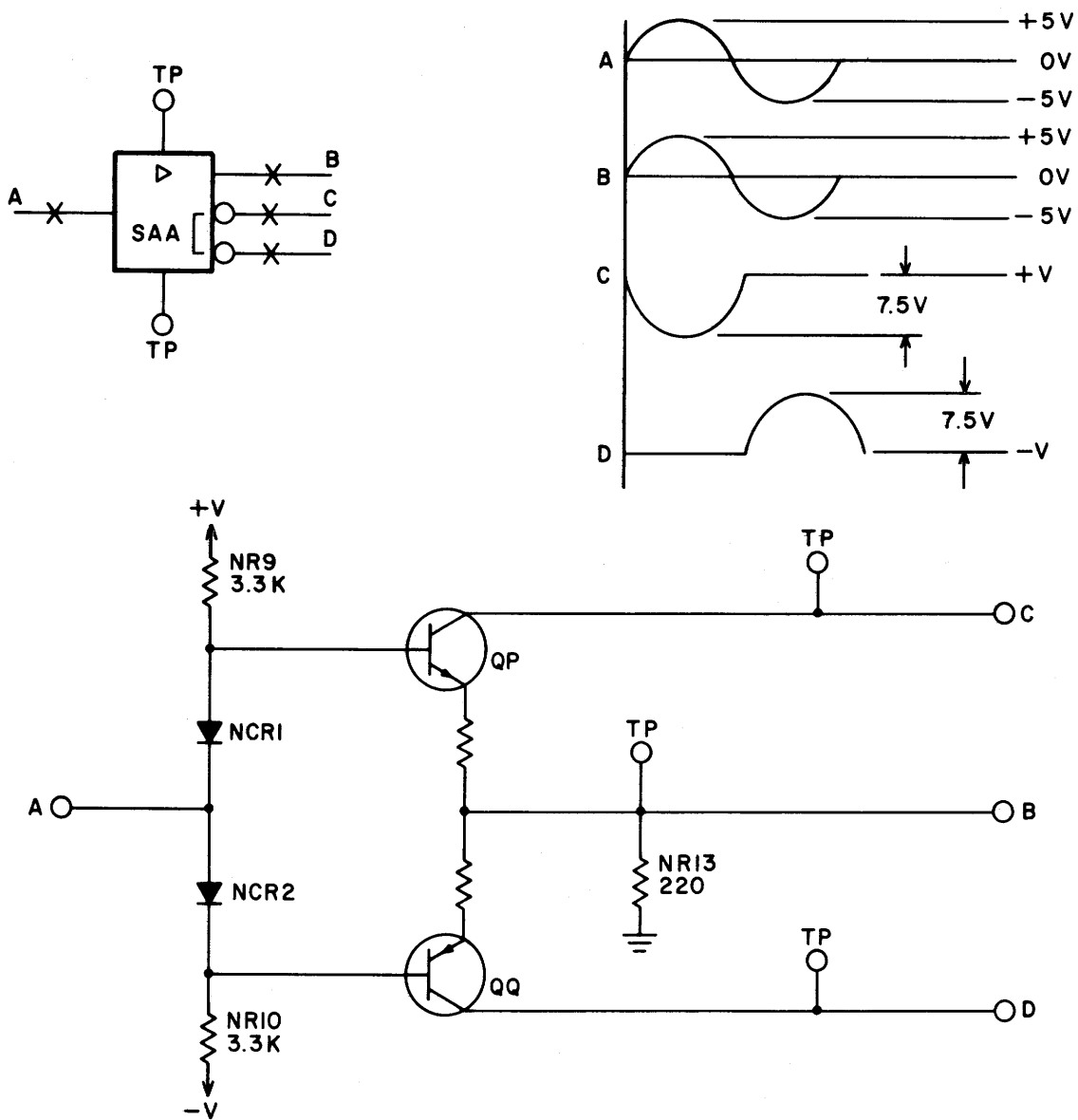
The information signal and the reference signal are transformer coupled to a matched diode bridge network by transformers NT1 and NT2, respectively. Resistors NR5, 6, 7, and 8 are selected to null out any mismatch in the bridge diodes or the other bridge resistors.

An output filter, NL1 and NC1, rejects the unwanted 50 kHz reference signal at the output of the circuit.

When the input signal across A and B is nulled, the bridge is unbiased and current flow depends on the polarity of the NT2 secondary. If the top of the winding is positive relative to the bottom, current flows from the bottom of the winding through CRNA, NR1, NR2, and CRNC back to the top of the winding. If the polarity is opposite that previously stated, current flows from the top of the winding through CRND, NR4, NR3, and CRNB returning to the bottom of the winding. In either case, output D is at 0 ± 4 mv.

When the signal at A and B becomes in phase with the reference signal at C, the bridge is biased in the positive direction. This state reduces current flow through NR2/CRNC and NR3/CRNB which unbalances the NT2 secondary halves and causes the center tap (and circuit output D) of the NT2 secondary to go positive. As the amplitude of the input signal increases, the increasing bridge bias drives the circuit output more positive.

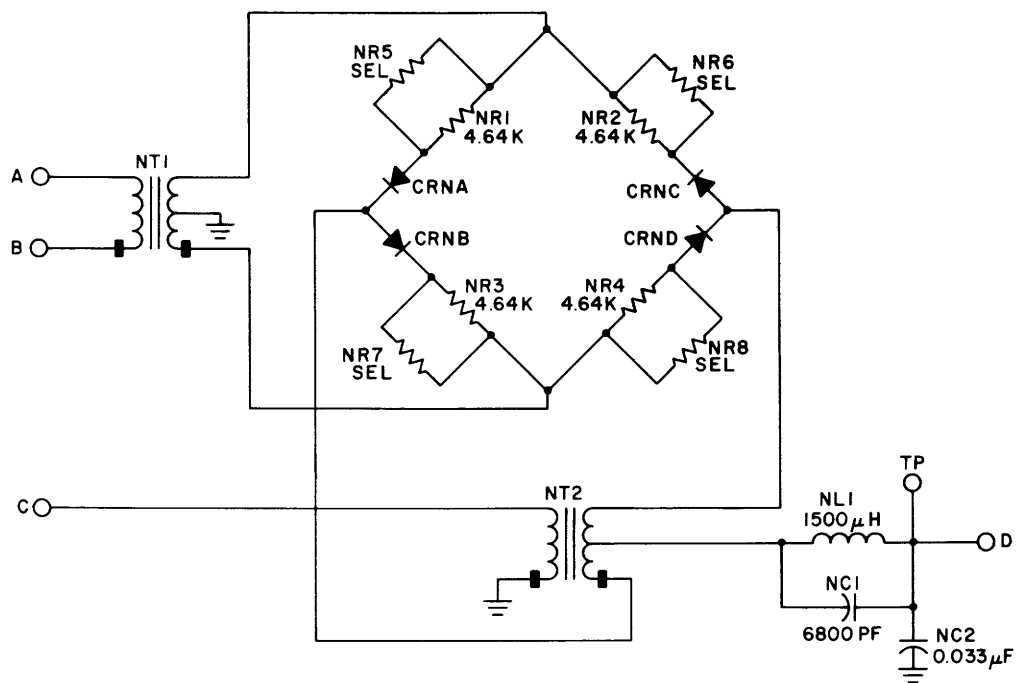
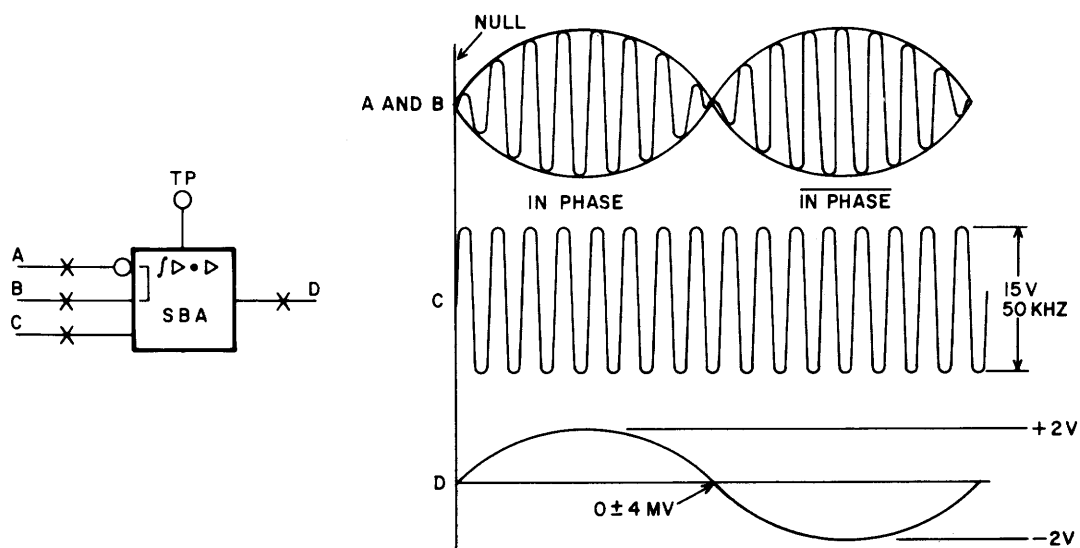
A signal at A and B that is out of phase with reference signal C, biases the bridge in the negative direction. Now current flow through NR1/CRNA and NR4/CRND legs is reduced. Again the NT2 secondary halves are unbalanced, but in this case the center tap goes negative. As before the output amplitude increases and decreases with the amplitude of the input signal.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

6T140

Figure 7-40. Bipolar Current Buffer - SAA



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

6T141

Figure 7-41. Demodulator - SBA

Attenuator - SBB/SBD

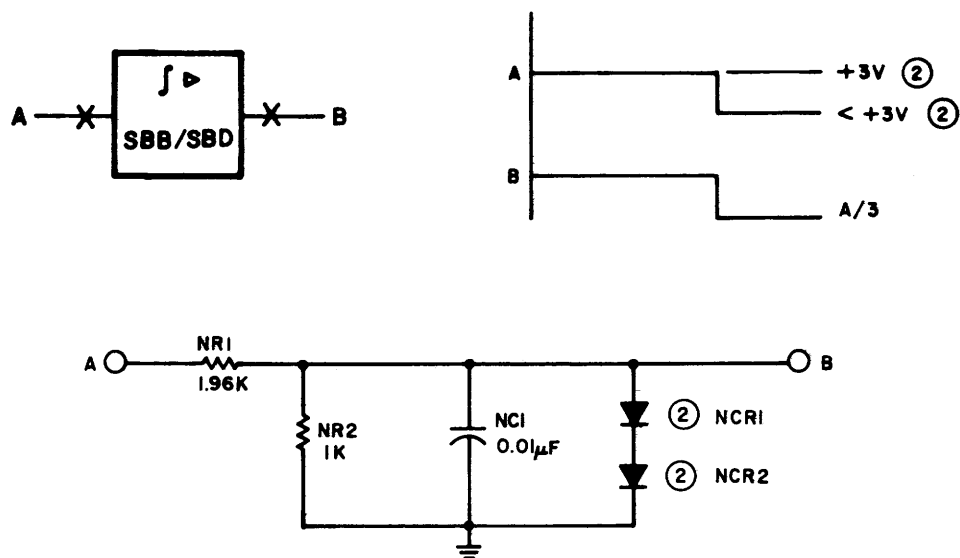
The SBB and SBD circuits (Figure 7-42) reduce the input voltage present at A by a factor of 3, approximately.

Capacitor NC1 filters the output voltage from voltage divider resistors NR1 and NR2. Series diodes NCR1 and NCR2 limit output B to a maximum of 1.6 volts. This limiting protects circuits driven by output B in the event of an abnormally high voltage being present at A. During normal operation, the diodes are nonconductive.

Voltage Divider - SBE/SBF

The SBE and SBF circuits (Figures 7-43) provide reference voltage outputs (0.744 volts SBE, 0.589 volts SBF) at A that are independent of normal variations in the 5-volt supply.

Resistor NR1 provides the zener diode NVR1 with approximately 20 ma from the 5-volt supply. This results in a very stable 3.6 volt reference. Resistors NR2 and NR3 divide the 3.6 volts to produce the desired ratio at output A. Capacitor NC1 filters the output.

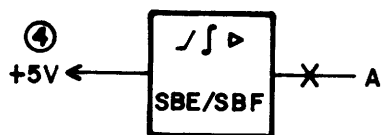


NOTES:

- 1 VOLTAGE AND COMPONENT VALUES FOR REFERENCE ONLY
- ② POLARITY REVERSED IN SBD CIRCUIT TYPE

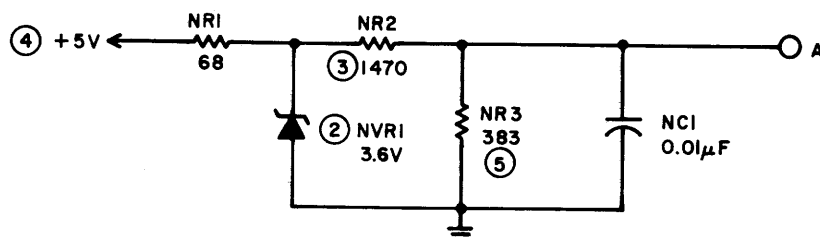
6T154

Figure 7-42. Attenuator - SBB/SBD



A = +0.744V FOR SBE

A = -0.589V FOR SBF

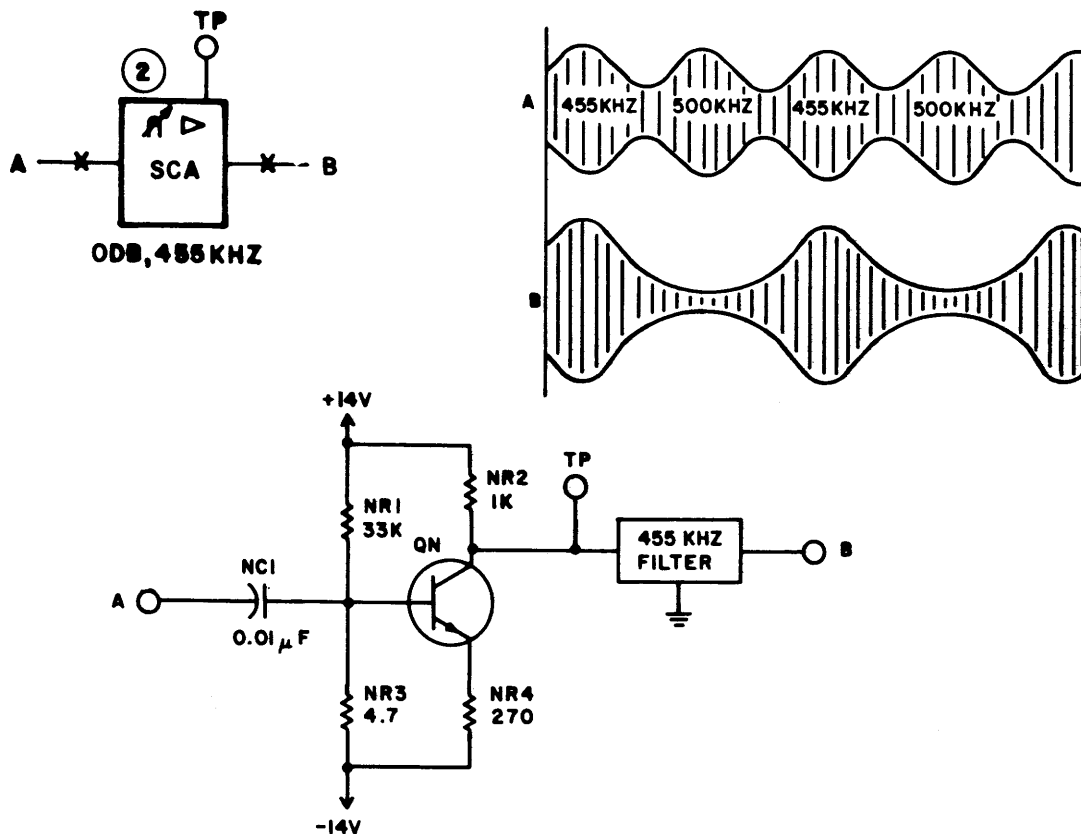


NOTES:

1. VOLTAGE AND COMPONENT VALUES FOR REFERENCE ONLY
- (2) POLARITY REVERSED IN SBF CIRCUIT TYPE
- (3) VALUE IS 1780 OHMS IN SBF
- (4) -5V IN SBF
- (5) VALUE IS 348 OHMS IN SBF

6T151

Figure 7-43. Voltage Divider - SBE/SBF



NOTES:

1. VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.
- ② ADJUSTABILITY ARROW REFERS TO BALANCE POTENTIOMETER CONNECTED TO INPUT A.

6T164

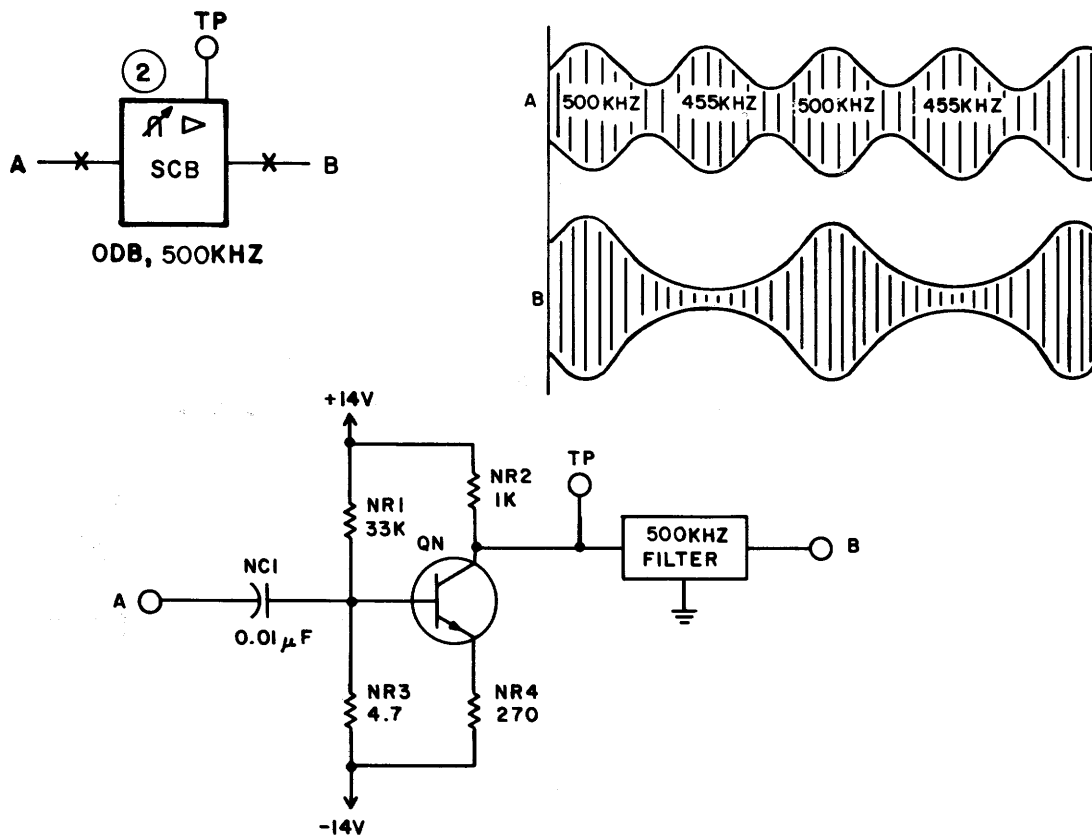
Figure 7-44. Filter - SCA

Filter - SCA

The SCA circuit (Figure 7-44) amplifies and passes the 455 kHz component of the track servo signal, and blocks passage of the other signal component (500 kHz).

The circuit consists of a transistor voltage amplifier with a gain of 4.4 db and a ceramic, ladder-bandpass filter with an insertion loss of 4 db (max). As a result the signal incurs no voltage loss in the circuit.

The bandwidth at the -1 db point (relative to the center frequency attenuation) is 20 kHz minimum, at -2 db it is 30 kHz minimum, at -6 db it is 40 kHz minimum, and at -60 db it is 72 kHz maximum.



NOTES:

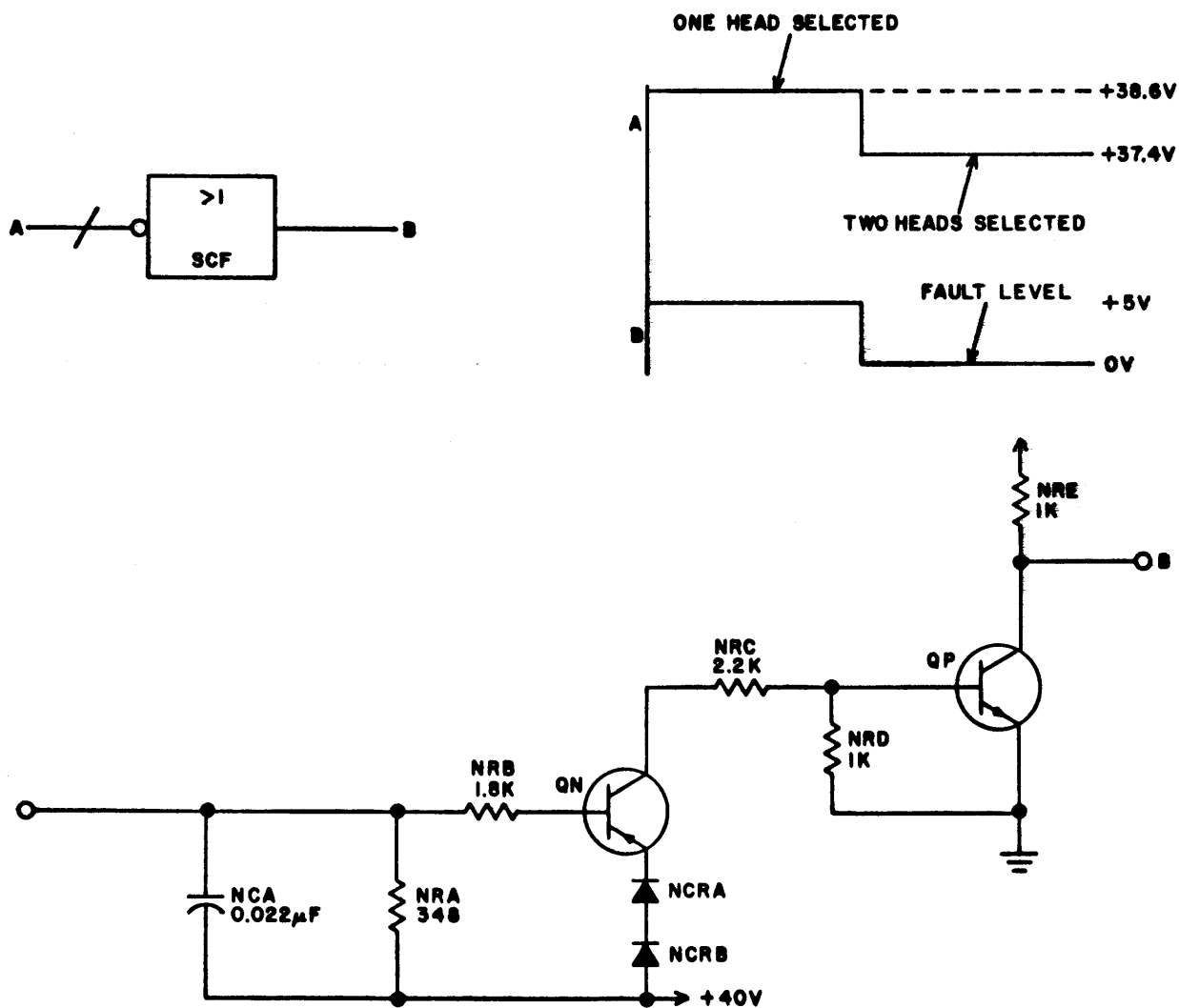
1. VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.
- ② ADJUSTABILITY ARROW REFERS TO BALANCE POTENTIOMETER CONNECTED TO INPUT A.

6T165

Figure 7-45. Filter - SCB

Filter - SCB

The SCB circuit (Figure 7-45) is identical to the SCA circuit except that it passes the 500 kHz component of the track servo signal and blocks the 455 kHz component.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7K30

Figure 7-45. 1. Multiple Head Select Detector - SCF

Multiple Head Select Detector - SCF

The SCF circuit indicates +5 vdc at output B when no more than one head is selected. If two or more heads are selected, output B is 0 vdc.

Capacitor NCA filters transient voltages preventing a false indication of more than one head selected. Diodes NCRA and NCRB provide a voltage bias on the emitter of QN. Resistors NRA and NRB are a voltage divider network.

Input A is fed by all heads, each through 10K of resistance. When one head is selected, only one 10K resistor goes to ground through a head select transistor. The current flow through NRA will not cause sufficient voltage drop across NRB to forward bias QN.

When two or more heads are selected, two or more 10K resistors are switched to ground. This causes increased current through NRA. The voltage drop across NRB then decreases enough to forward bias QN. QN turns on, passing collector current through NRC into the base of QP. QP turns on, bringing output C from +5 vdc to 0 vdc.

Delay - UB

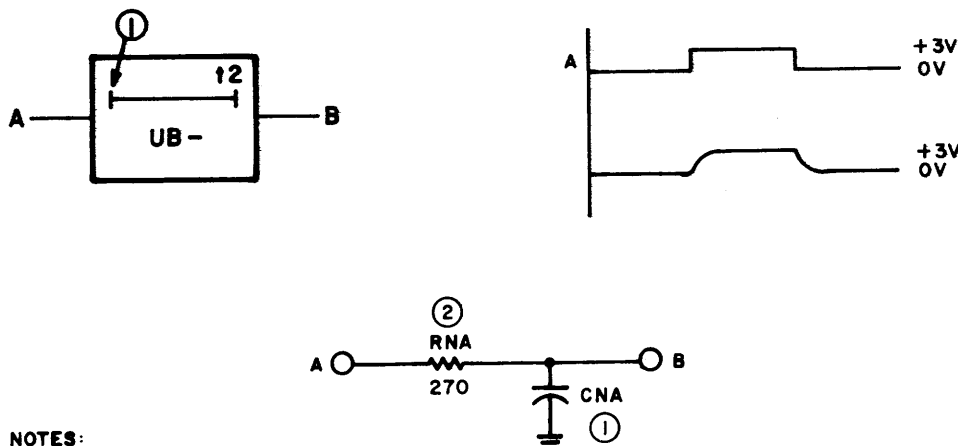
The capacitor delay circuits (Figure 7-46) delay a "1" input at A for a specified period of time before providing a "1" output at B. Delay time for a "0" pulse is negligible.

Assume a "0", ground, enters at A. If the capacitor is discharged, it remains discharged and the output remains "0". If the capacitor is charged when the "0" signal appears, the capacitor discharges almost instantaneously, and the "0" appears with no noticeable delay.

If a "1", +3 volts, enters A while the capacitor is discharged, the capacitor must first charge to a minimum "1" voltage before a "1" can appear at B. The required charge time is the delay time of the circuit. The charge time is dependent on the capacitor value, the resistance between the source voltage and the capacitor, and the minimum voltage required to produce a "1" output.

Delay times for capacitive delays used in the DSU are as follows:

Delay type	Time
UBD	200 nsec
UBE	0.5 ms
UBF	0.2 ms



NOTES:

- ① VARIES WITH TYPE
- ② NOT USED ON UBF

6T155

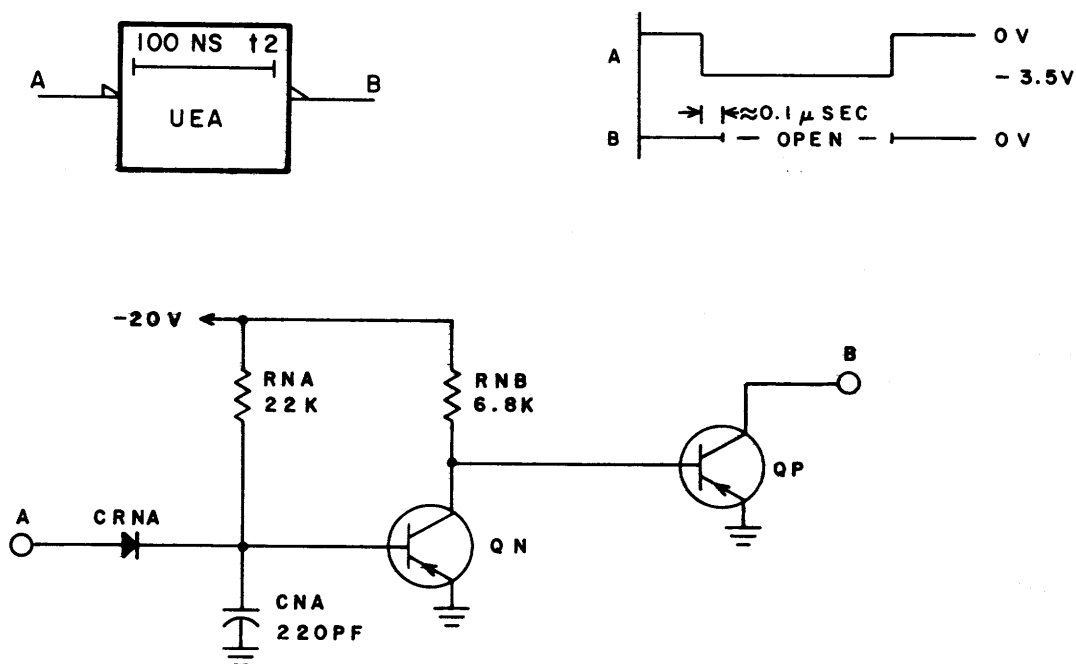
Figure 7-46. Delay - UB

Unidirectional Time Delay - UEA

The UEA circuit (Figure 7-47) provides a $0.1\text{-}\mu\text{sec}$ delay between the time that a -3.5v signal appears at A and the time that transistor QP turns off. Output at B is either ground or an open circuit.

When input A is near ground, QN is off. Transistor QP is on. The output is ground.

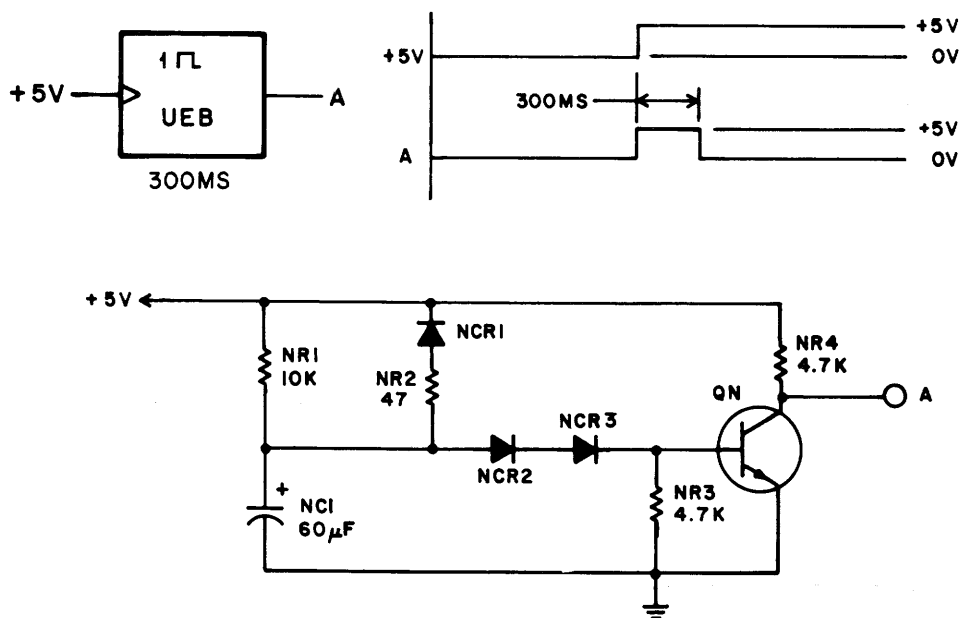
When input A goes to -3.5v , capacitor CNA begins charging. After $0.1\text{ }\mu\text{sec}$ the base of QN is sufficiently negative to turn QN on. Transistor QP turns off. The output is an open circuit.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

6T116

Figure 7-47. Unidirectional Time Delay - UEA



NOTE:

VOLTAGE AND COMPONENTS VALUES ARE FOR REFERENCE ONLY.

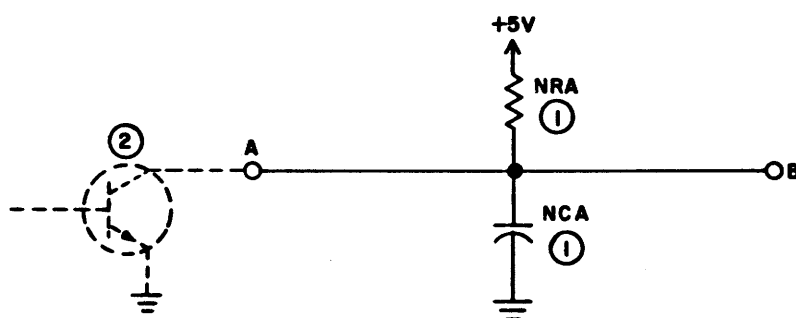
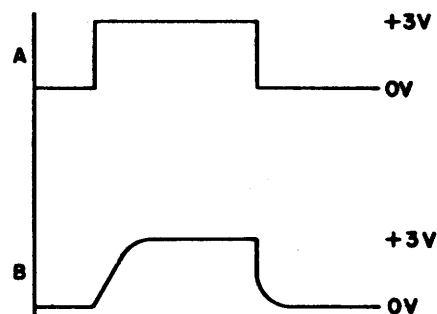
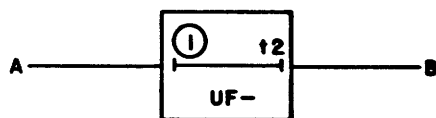
67159A

Figure 7-48. Delay - UEB

Single Shot - UEB

The UEB circuit (Figure 7-48) is a single shot that holds a clear signal on the units Fault register for 300 ms after +5 volts becomes available.

The circuit delay characteristic occurs as NC1 charges through NR1 to a threshold voltage of 2.1 vdc (determined by NCR2, NCR3, and base-emitter junction of QN). Resistor NR2 and diode NCR1 provide a quick discharge path for NC1 when +5 volts drops. The presence of this path ensures a short recycle period for transient off/on application of the +5 vdc.



- NOTES: ① VALUE DEPENDENT ON CIRCUIT TYPE
② OPEN COLLECTOR TRANSISTOR IN PRECEDING STAGE

7K36

Figure 7-48.1. Delay - UF-

Delay - UF-

The UF- delay circuit is used to delay open collector integrated circuits. The circuit delays a "1" input before providing a "1" output at B. The delay time for a "0" pulse is negligible. The delay circuit consists of a resistor connected to +5v and a capacitor connected to ground.

Assume that a "0" (ground) enters at A. If the capacitor is discharged, it remains discharged. The output is an immediate "0". If the capacitor is charged when the "0" signal enters, it discharges almost instantaneously. The "0" appears at output B with no noticeable delay.

If a "1" (+3.0v) enters at A, and the capacitor is discharged, the capacitor must first charge to a minimum "1" voltage (typically +0.7v) before the "1" appears at output B. The time necessary to charge the capacitor to this minimum voltage is the delay time of the circuit. The charge time is dependent on the value of the capacitor, the value of the resistor, and the minimum voltage required to produce a "1" response.

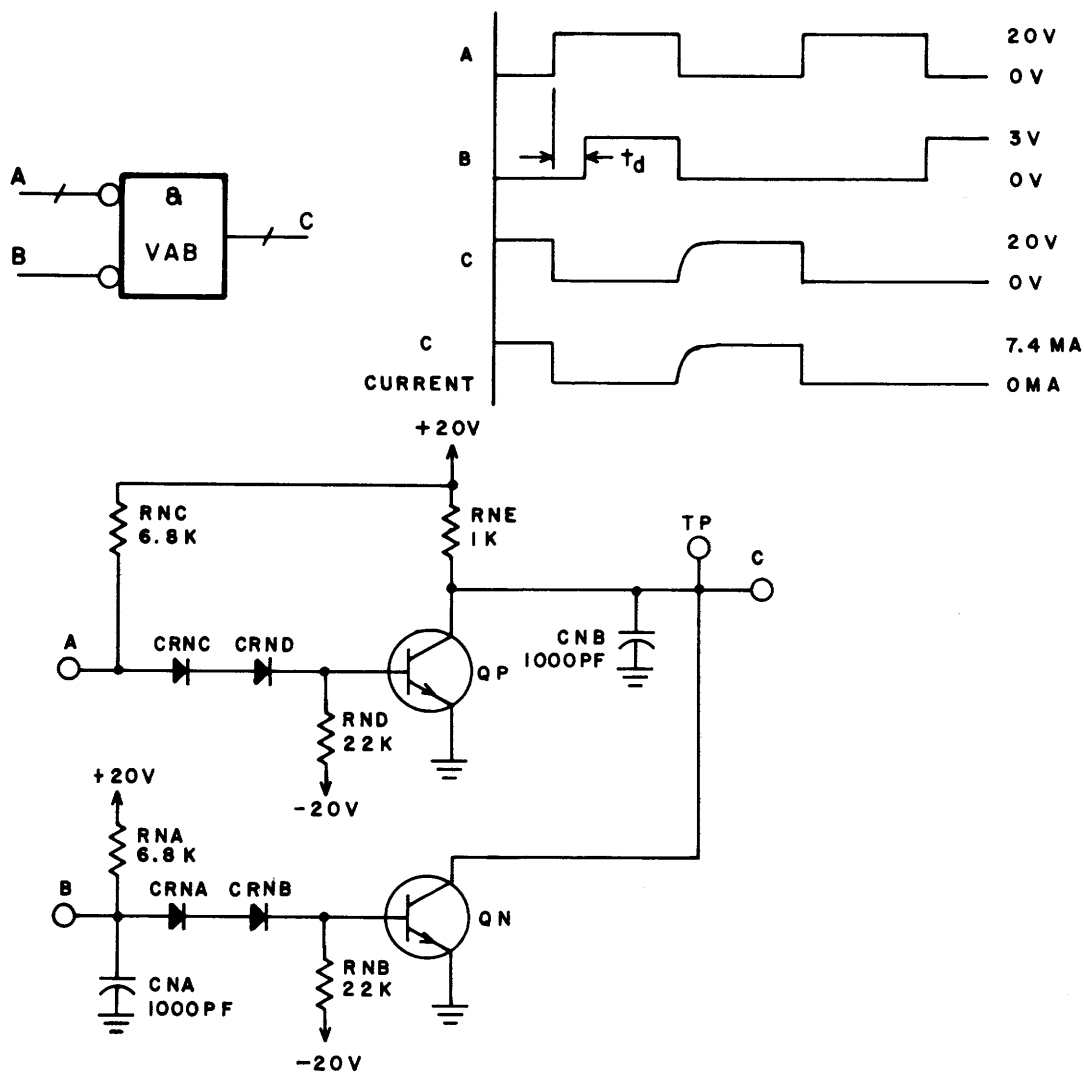
Delay Type	Time
UFA	1.3 μ sec
UFB	0.5 μ sec
UFC	0.2 μ sec
UFD	6.0 μ sec

And - VAB

The VAB circuit (Figure 7-49) consists of two silicon peripheral logic inverters whose outputs share a common load resistor, RNE. When both inputs A and B are "0" (ground), the output at C will be a "1" (+3v). If either or both of the inputs are a "1", the output at C will be a "0". This is an AND gate for zeroes, or a NAND function.

When both A and B are at ground, QN and QP are off. The output at C is supplied from the +20v source through RNE. The output is a positive voltage, representing a non-logical "1". If input A experiences a positive voltage while B is at ground, QP turns on and conducts current from the +20v supply through RNE to ground. The "0" on B has no effect, as all the supply voltage is tapped to ground. The output at C is ground, or a "0". The situation is similar if A is "0" and B is "1". The output is "0". If both A and B have positive voltage applied to them, QN and QP both conduct. The output is "0".

Capacitors CNA and CNB provide a one's delay on input B and output C, respectively. They also maintain a noise barrier to isolate the circuit from stray pulses on the lines.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

6T117

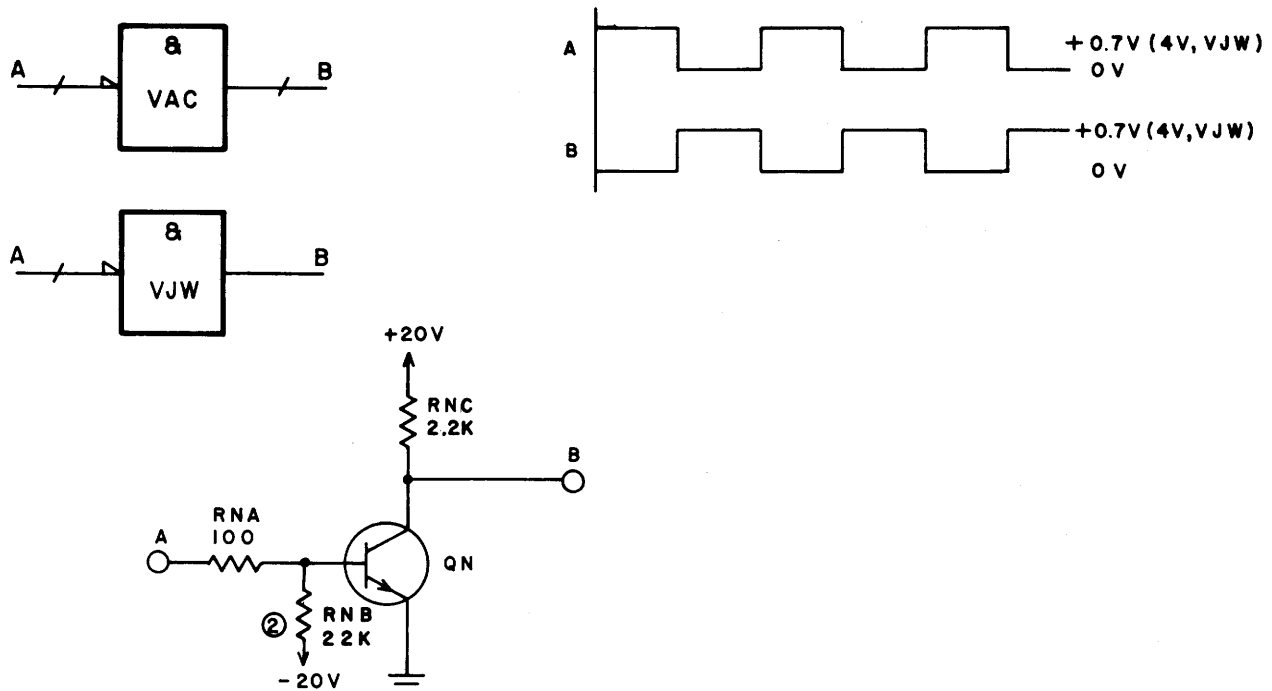
Figure 7-49. And - VAB

And/Or (Single Input) - VAC, VJW

The single input AND/OR or silicon peripheral logic (SPL) inverter (Figure 7-50) provides an inversion from input A to output B: A "1" on A produces a "0" on B, or a "0" on A produces a "1" on B. The inverter's output may be connected to the output of other inverters to form NAND functions or NOR functions.

The SPL inverter is a single NPN silicon transistor connected as a common emitter amplifier. When A is a "0" (between 0v and +0.3v) the transistor is off. This allows current to flow from the +20v supply, through RNC to output B. The output is a "1". When input A is a "1" (between +0.7v and +3.0v) the transistor turns on. The transistor conducts current from the +20v source, through RNC to ground. This leaves output B near ground, or a "0".

Since the base-emitter threshold for a silicon transistor is approximately +0.7v, the circuit ignores up to 0.5v of transient noise.



NOTES:

1. VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.
- ② DOTTED LINE TO -20V AND RESISTOR RNB FOR VJW ONLY.

6T118

Figure 7-50. And/Or (Single Input) - VAC, VJW

If the circuit drives just one other transistor, the output may be connected directly to the base of the driven transistor. For a fan-out of 2 or more, a base isolation resistor is required for each driven transistor. This resistor ensures that the base drive provided to each of the driven transistors will be nearly independent of differences in base-emitter voltages. For a fan-out of 2 the collector load resistor must be reduced by one-half its value for driving one transistor to provide for the additional voltage drop across the isolation resistors.

Switching time for an inverter with a fan-out of 1 is typically 15 nsec.

Power Driver - VJK

The VJK circuit (Figure 7-51) is similar to the VJS circuit with the addition of capacitor CNB and two outputs. CNB slows the switching time of QN and provides a ramp output. Output B connects to the center tap of the head. Output C contains a 10K resistor and is connected to a voltage supply in a fault detect circuit. If two heads are selected the effective resistance falls to 5K (two 10K resistors in parallel). The increase in current causes a Fault signal. Output D contains a diode that isolates each Write Gate.

Power Driver - VJL

The VJL circuit (Figure 7-52) is a gate used to bias an analog gate.

If +20v appears at A, QN turns on. The base of QP goes to ground. Transistor QP is off. Capacitor CNA charges through RND to +20v. Output at B is a ramp to +20v.

A +0.2v signal at A turns QN off. When QP turns on, the collector voltage of QN clamps at +0.7v. CNA discharges rapidly through QP. Output B drops to ground.

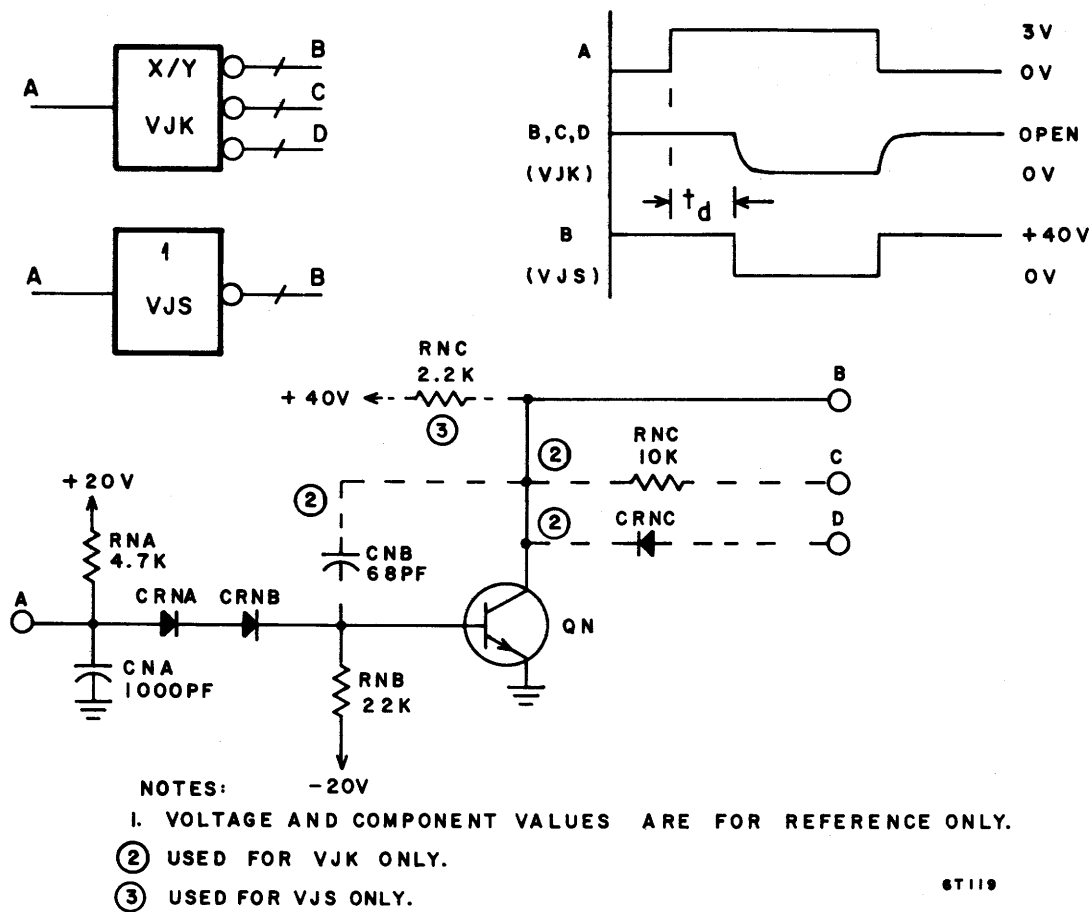
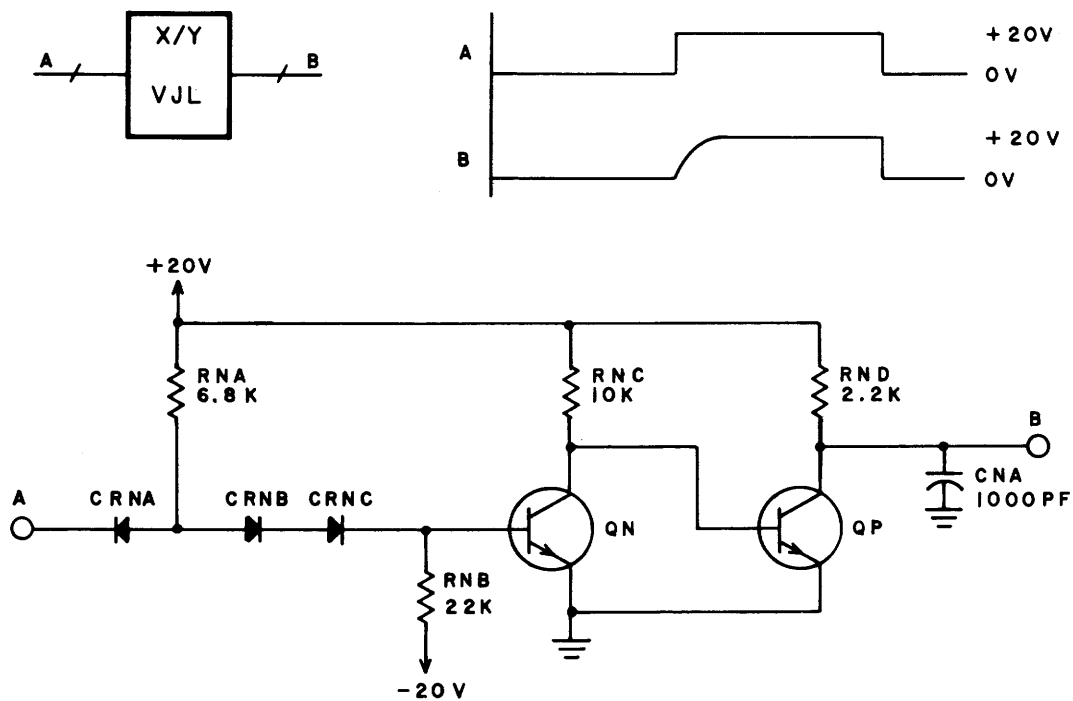


Figure 7-51. Power Driver - VJK, VJS



6T120

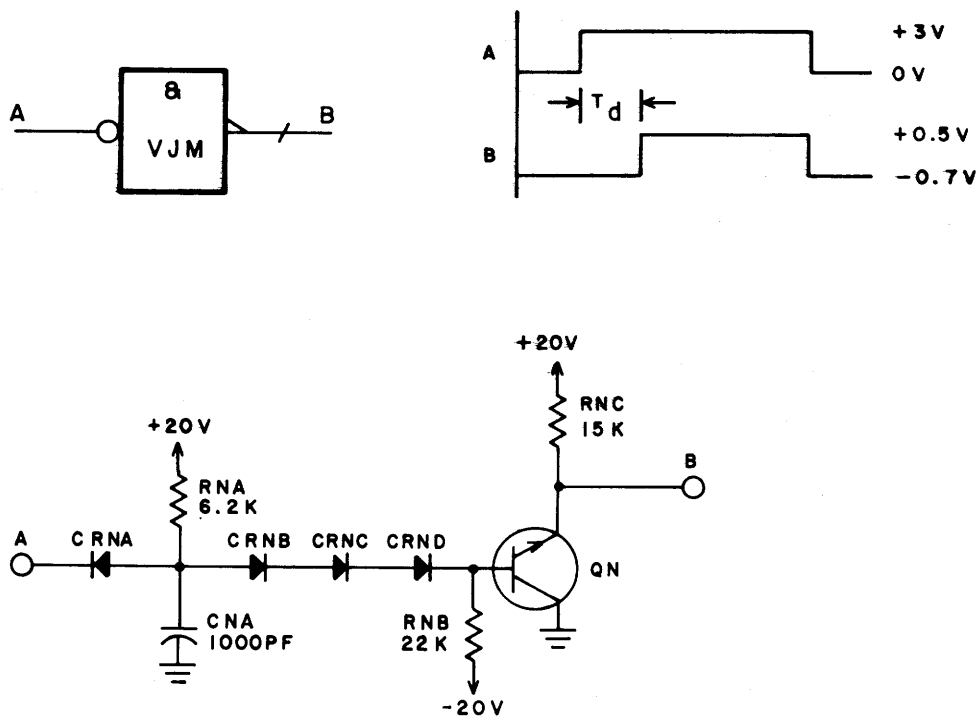
Figure 7-52. Power Driver - VJL

And - VJM

The VJM circuit (Figure 7-53) gates a particular receiver into operation. A "0" input at A results in an "open" enable signal to the receiver. A "1" input at A disables the receiver.

A "0" (0v) input forward biases diode CRNA. The +20v supply current is drawn through RNA and CRNA, leaving the base of QN reverse biased. Transistor QN is off. Output is held at -0.7v by the next stage.

A "1" input turns QN on. The output goes to ground. No receiver signal can pass into the receiver.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

6T121

Figure 7-53. And - VJM

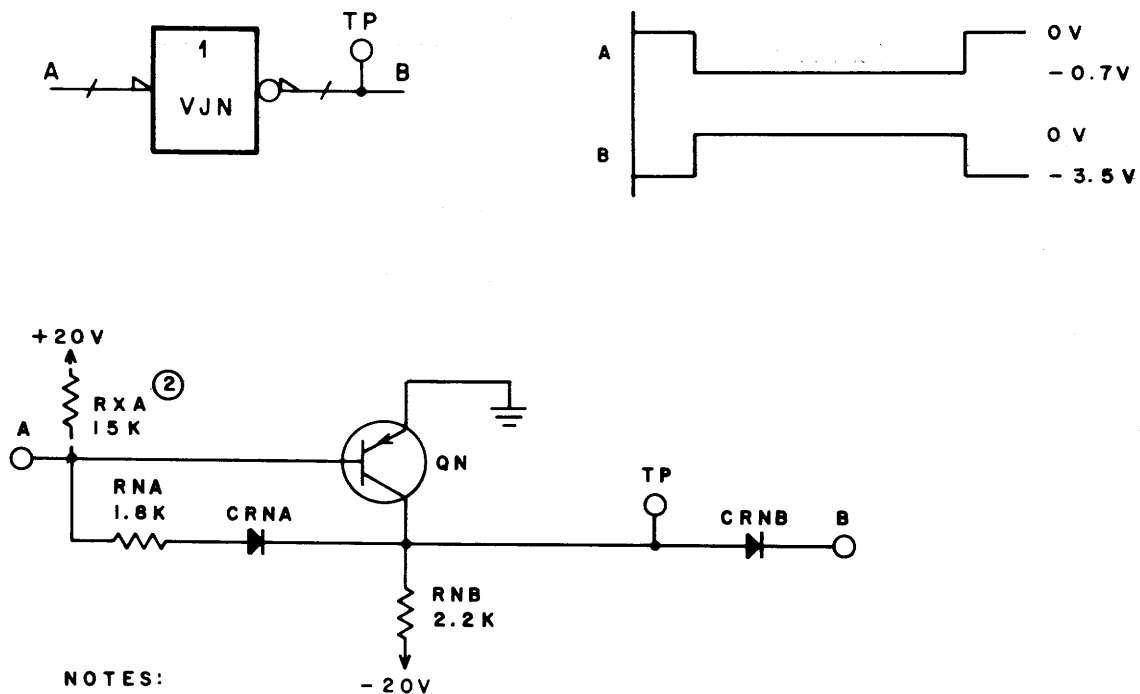
Or - VJN

The VJN circuit (Figure 7-54) is a NAND circuit that inverts the input signal. Input A is connected to the output of a receiver and to a gating circuit. If the Write gate is off, the base of QN is grounded. The circuit is disabled.

When the write gate is on, QN turns on and the receiver inputs a "0". Transistor QN turns on further and goes into saturation. Output voltage at B is approximately -0.2v.

When the receiver inputs a "1", QN comes out of saturation. Output at B is approximately -3.5v.

Whenever the write gate is on, QN is on to some degree. Only when the write gate is off is the base of QN at ground and QN off.



NOTES:

1. VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

② RESISTOR AND POWER SUPPLY EXTERNAL TO VJN.

6T122

Figure 7-54. Or - VJN

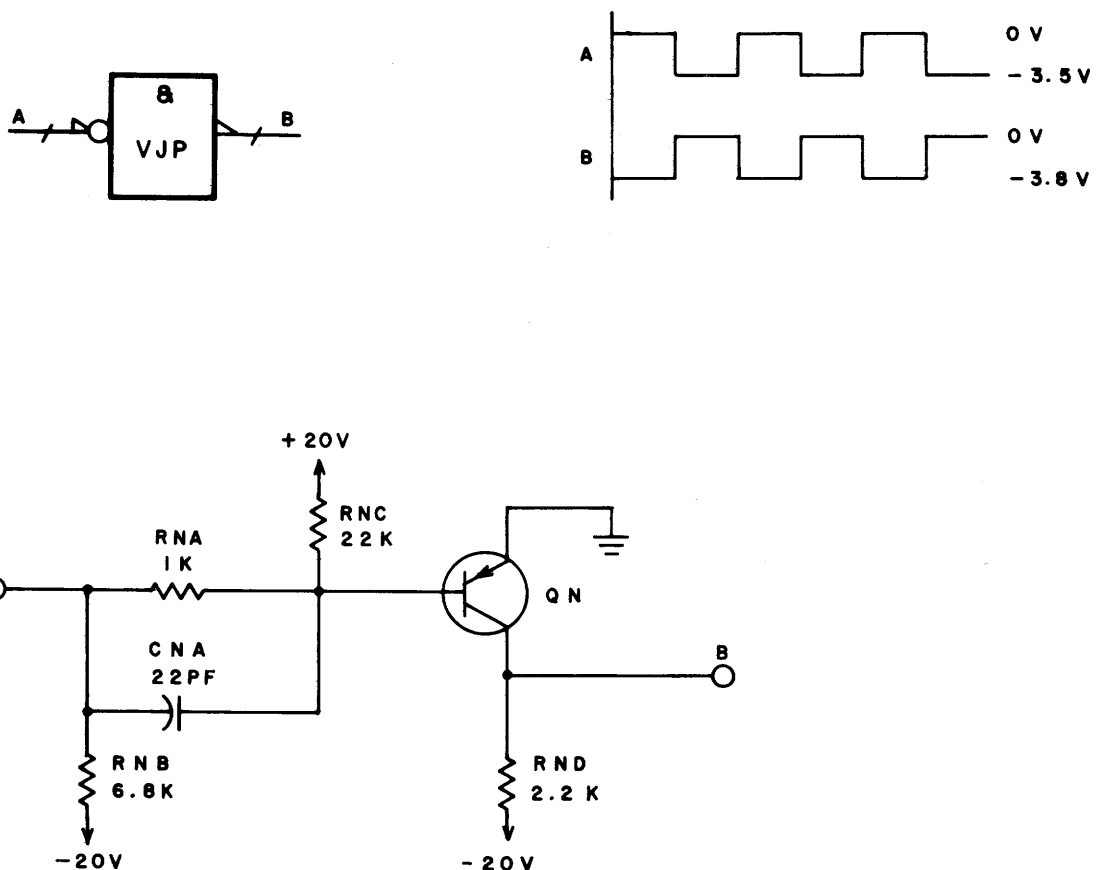
And - VJP

The VJP circuit (Figure 7-55) is normally used as the input circuit to a toggle flip-flop. It ties two receiver outputs to a single-ended output. Capacitor CNA is used to reduce the input impedance for faster switching.

When input A is near ground, the base of QN is at approximately +0.9v. Transistor QN is off. Output at B approaches -20v, but is clamped at -3.8v by a Zener diode in the following circuit.

When input A is -3.5v, QN turns on. Output drops to approximately -0.2v.

Input to A is short (100 nsec), negative, data pulses. Output B is also short pulses.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

6T123

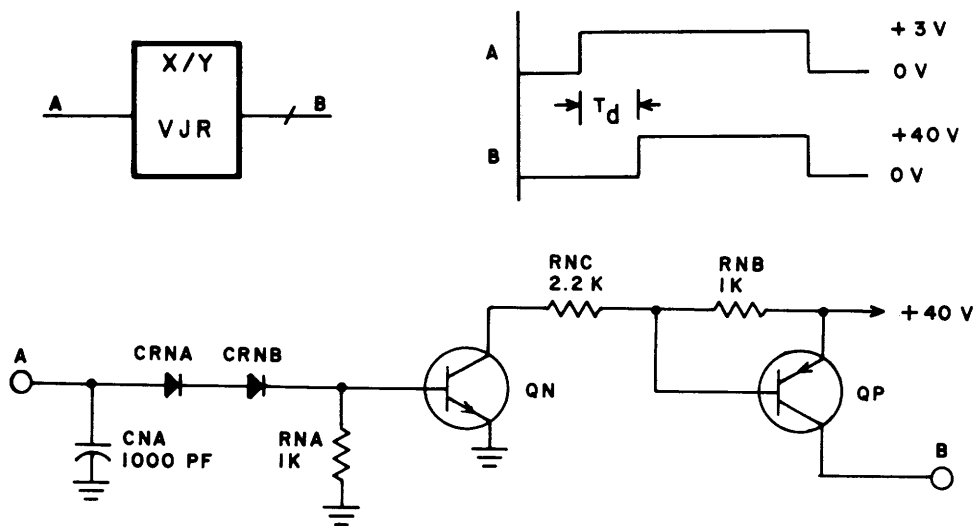
Figure 7-55. And - VJP

Power Driver - VJR

The VJR circuit (Figure 7-56) is a +40v switch. A "1" on input A produces +40v at output B. A "0" on input A stops current flow.

A "1" input turns QN on. Transistor QN conducts current from the +40v supply, causing a voltage drop across resistor RNB. This voltage drop turns on QP. Output B is at +40v.

A "0" input turns QN off. Since current no longer flows, the emitter and base of QP are at equal voltage. Transistor QP is off. Output B goes to ground.



NOTE:
VOLTAGE AND COMPONENT VALUES
ARE FOR REFERENCE ONLY.

6T124

Figure 7-56. Power Driver - VJR

Or - VJS

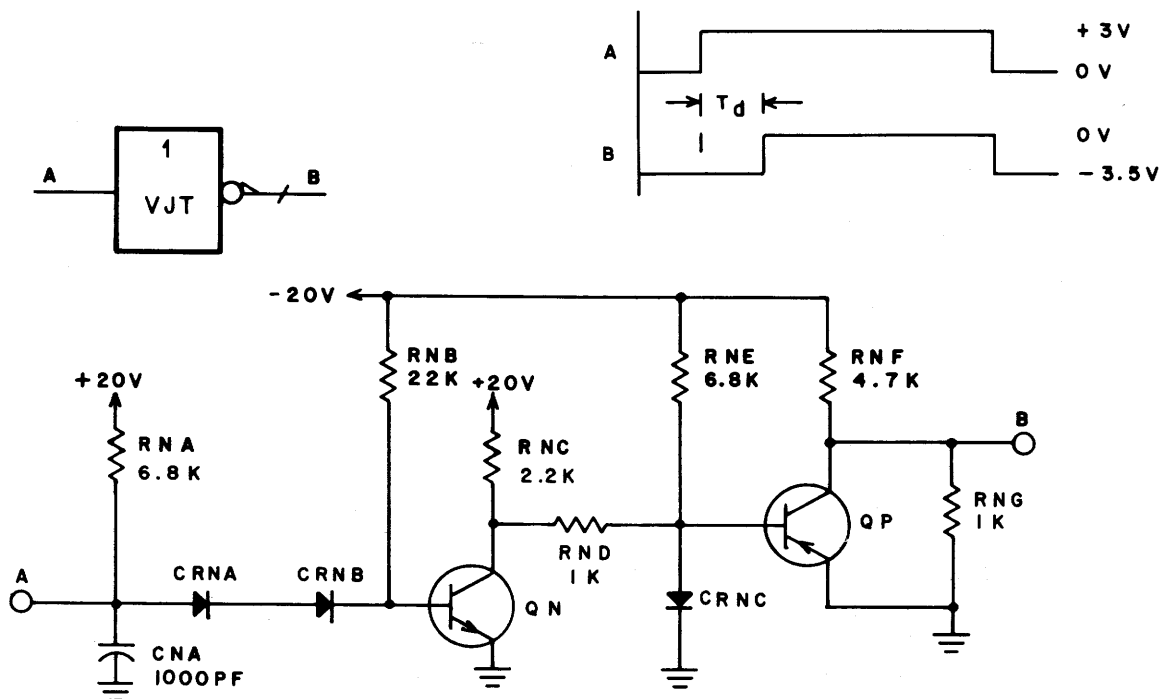
The VJS circuit (Figure 7-51) is a standard inverter with a capacitor delay at the input. A "1" at input A pulls the output at B to ground. A "0" produces a +40v output.

Or - VJT

The VJT Circuit (Figure 7-57) is a gate to the WBB toggle flip-flop. A "1" input at A produces a ground at B, which keeps the flip-flop off. A "0" input at A produces a -3.5v output at B, which releases the flip-flop and presets it in a given state.

When a "0" is applied to input A, the base of QN goes to ground. Transistor QN is off. The base of QP is clamped at +0.6v by diode CRNC. Transistor QP is off. Output B is -3.5v derived from the voltage dividing network of RNF and RNG.

When A goes to a "1", capacitor CNA charges. After a delay, the base of QN is positive enough to turn QN on. The base of QP goes negative through resistor RNE. Transistor QP turns on. The output at B drops to ground.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

8T125

Figure 7-57. Or - VJT

And - VJU, VJV

The VJU and VJV circuits (Figure 7-58) are functionally identical. They consist of a standard inverter circuit with a capacitive filter input. The capacitor also presents a delay.

A "1" on input A reverse biases diode CRNA. Capacitor CNA charges through RNA until it is clamped at about 3 diode voltages (approximately 2.1v). QN turns on. Output B falls to ground.

If input A is a "0", CNA discharges through CRNA. Transistor QN turns off. Output B rises to a "1" level due to the clamping by a Zener diode.

And Or - VJW

Refer to circuit description for circuit type VAC.

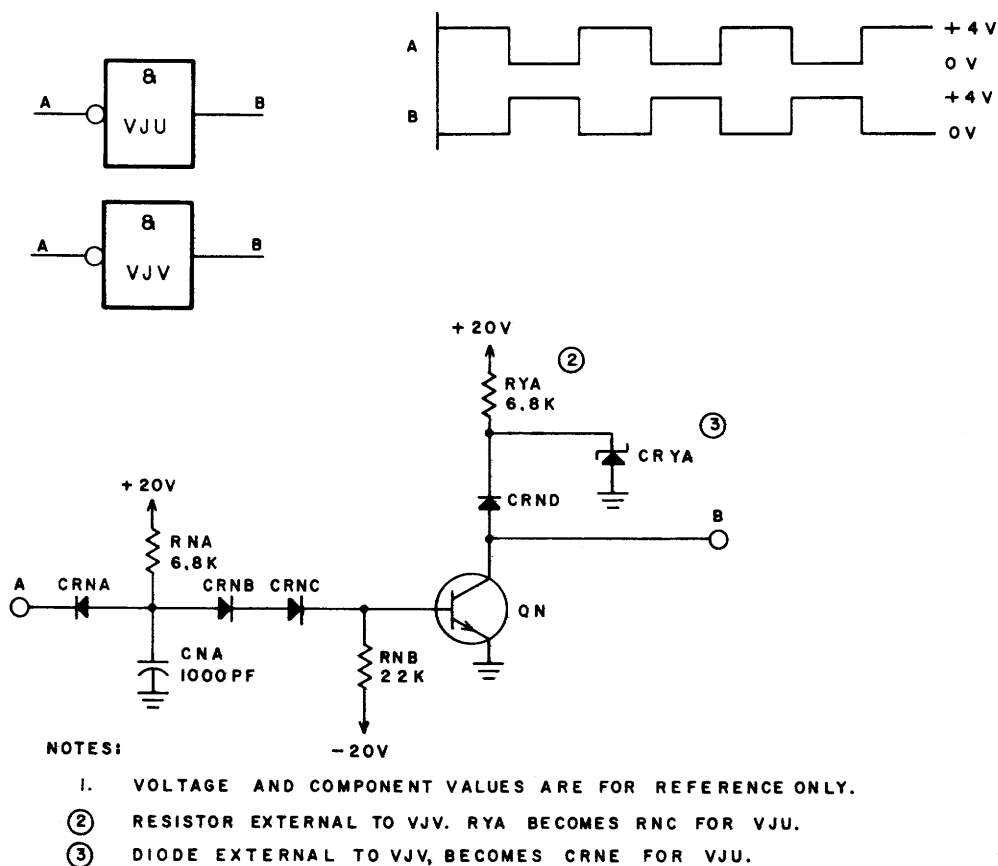
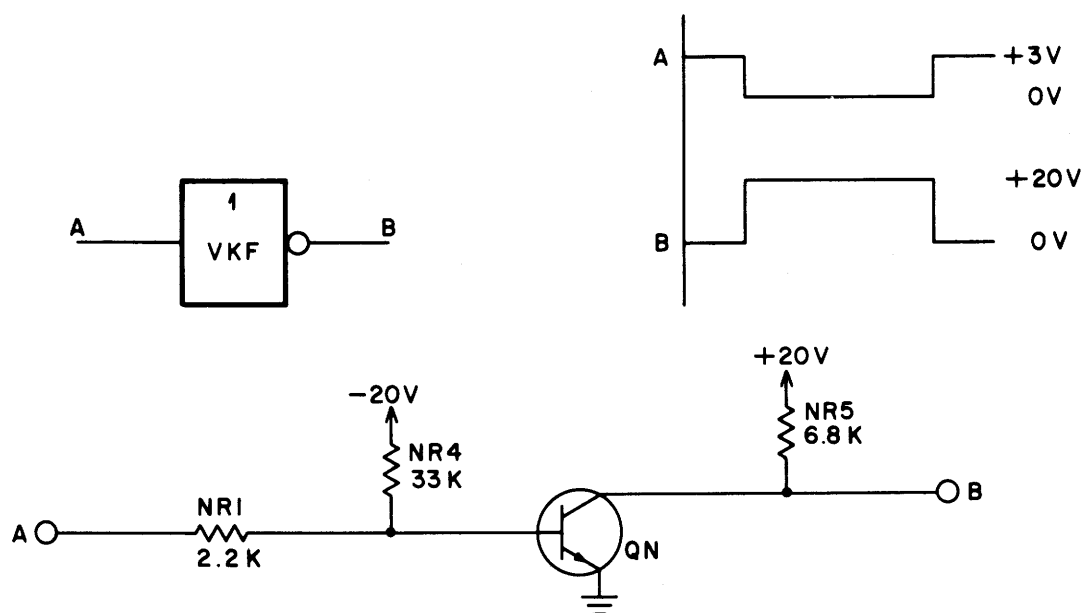


Figure 7-58. And - VJU, VJV

Inverter - VKF

The VKF circuit (Figure 7-59) is a simple digital inverter. It consists of a single NPN transistor in a common emitter configuration. A "0" at A turns QN off. This allows current to flow from the +20-volt supply, via NR5, and raise output B to a +20v level.

An input of "1" turns QN on. This directs current from the +20-volt supply through NR5 and QN to ground, leaving output B near a ground level.



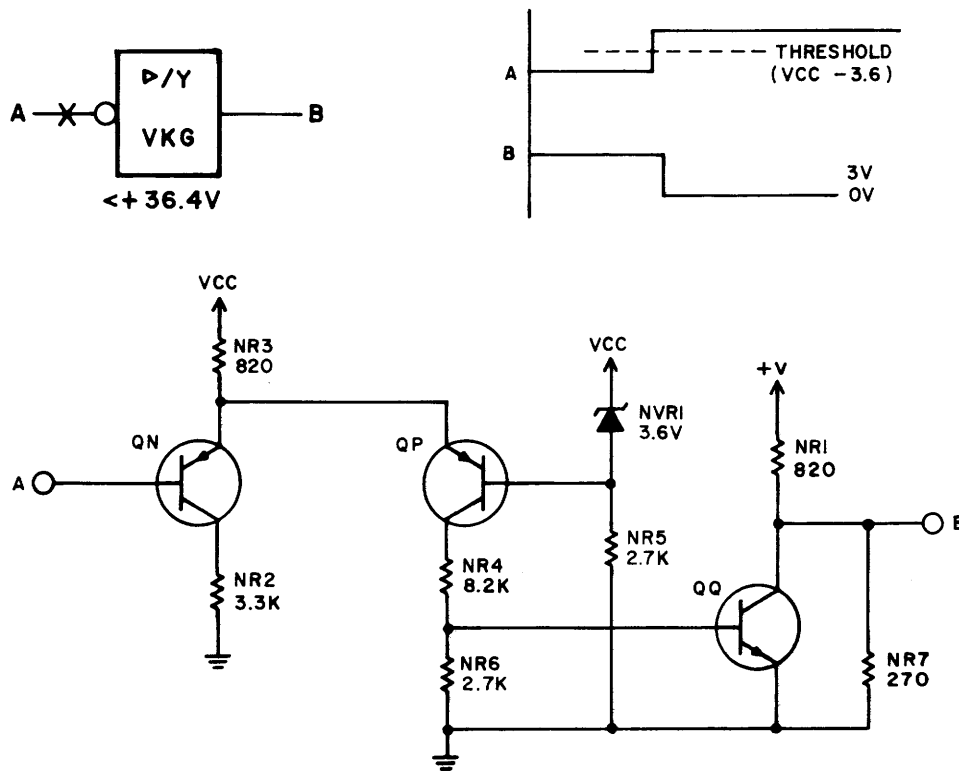
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

6T142

Figure 7-59. Inverter - VKF

Or Gate - VKG

The VKG circuit (Figure 7-60) detects the presence of write or erase current flow. When current flows, a voltage drop across an external resistor produces a voltage at input A that is lower than V_{CC} (+40 volts) less 3.6 volts. This acts to turn QN on and QP and QQ turn off to produce a "1" at B. If the current flow drops to a level that would impair the write operation, QN will turn off. This causes QP and QQ to turn on and a "0" to appear at B, indicating a fault.



NOTE:

1. VOLTAGE AND COMPONENT VALUES FOR REFERENCE ONLY

6T156

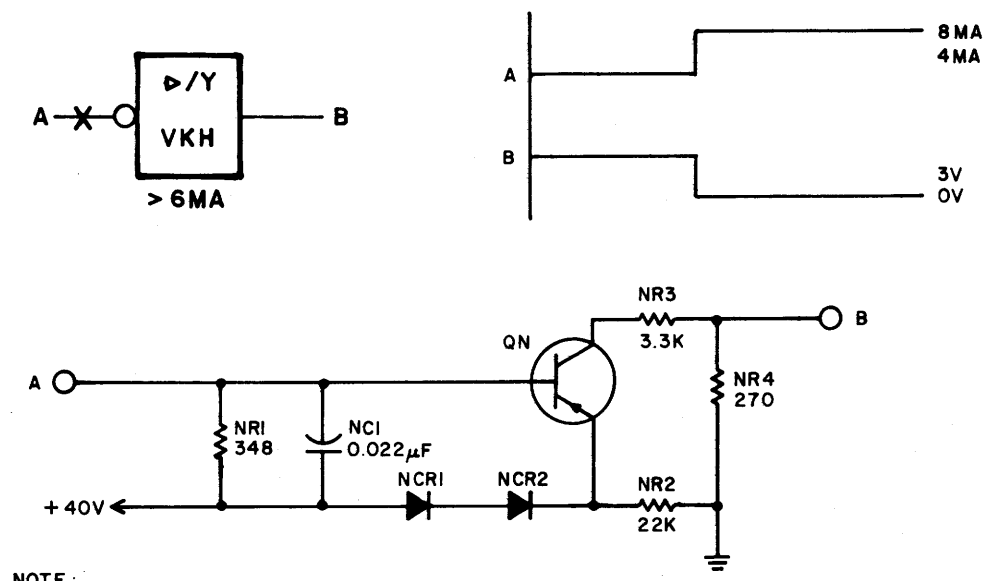
Figure 7-60. OR - VKG

Current Detector - VKH

The VKH circuit (Figure 7-61) detects the undesirable occurrence of multiple head selection.

Input A connects to the head select circuits. The selection of a head causes current to be drawn through resistor NR1. As long as a single head is selected, the voltage at the base of QN is insufficient to turn QN on. As a result, the circuit output, B, will remain at zero volts.

If more than one head is selected, the additional current flowing through NR1 causes QN to turn on. This produces a "1" at output B, indicating a fault.



NOTE:

I. VOLTAGE AND COMPONENT VALUES FOR REFERENCE ONLY

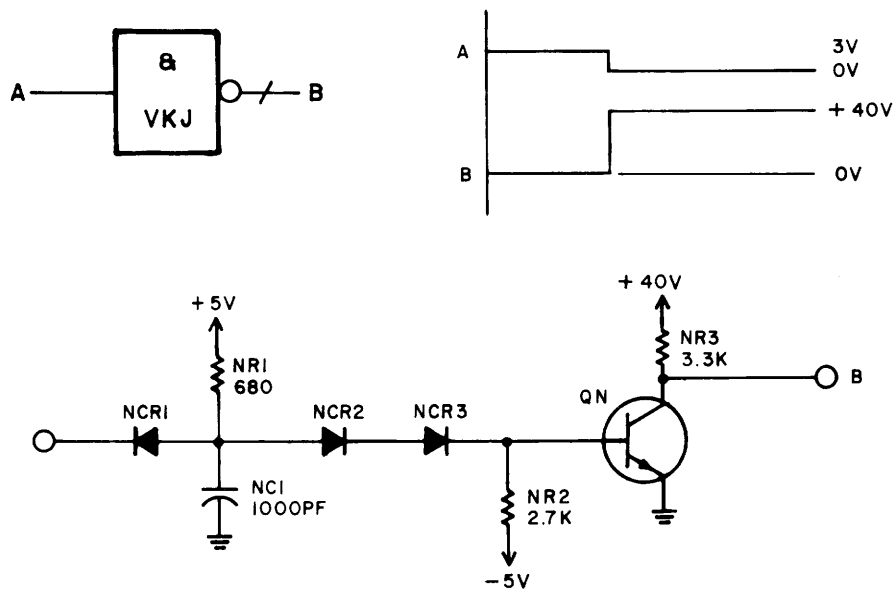
6T157

Figure 7-61. Current Detector - VKH

And Gate - VKJ

The VKJ circuit (Figure 7-62) guards against the write head receiving current except during a write operation.

When input A is a "0", QN is off and output B makes +40 volts available for write current. If the input is a "1", QN is off, output B approaches zero volts, and no write current is available to the write heads.

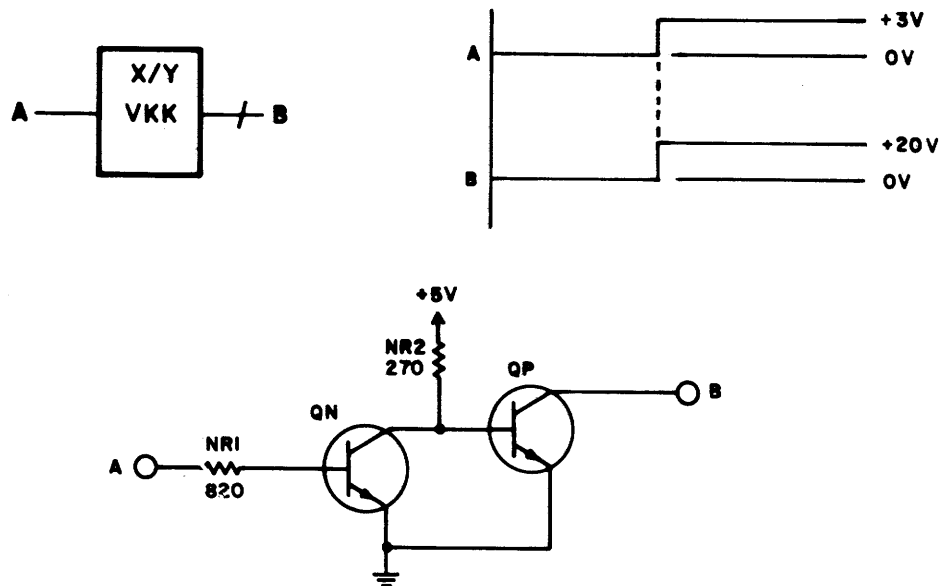


NOTE:

1. VOLTAGE AND COMPONENT VALUES FOR REFERENCE ONLY

6T149

Figure 7-62. AND - VKJ



NOTE:

VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

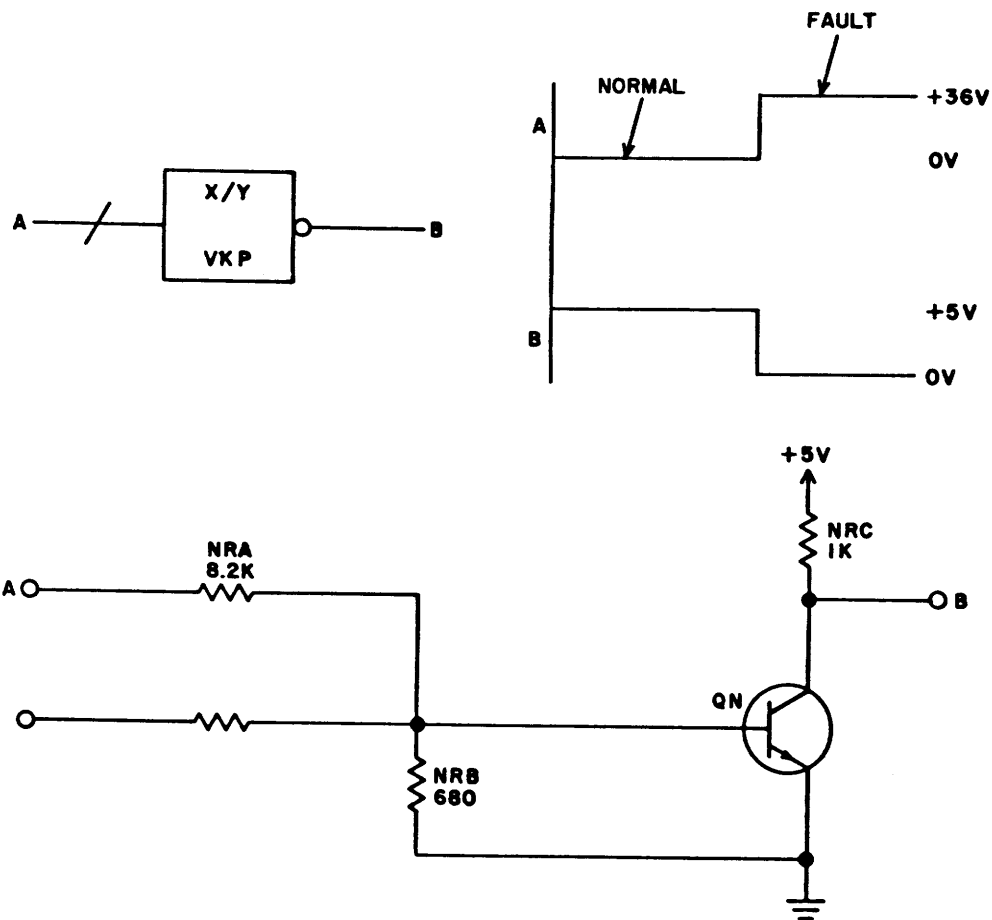
6T158

Figure 7-63. Solenoid Driver - VKK

Solenoid Driver - VKK

The VKK circuit (Figure 7-63) is a solenoid driver that operates under control of a TTL circuit. Circuit output B connects to one side of the solenoid coil with the other end of the coil connected to +20 vdc.

A logic "1" at input A turns transistor QN on pulling the base of QP to ground. With transistor QP off, output B is at +20 volts and the solenoid armature is de-energized. A logic "0" at input A turns QN off causing QP to conduct and output B to go to ground. The presence of a ground at B energizes the solenoid.

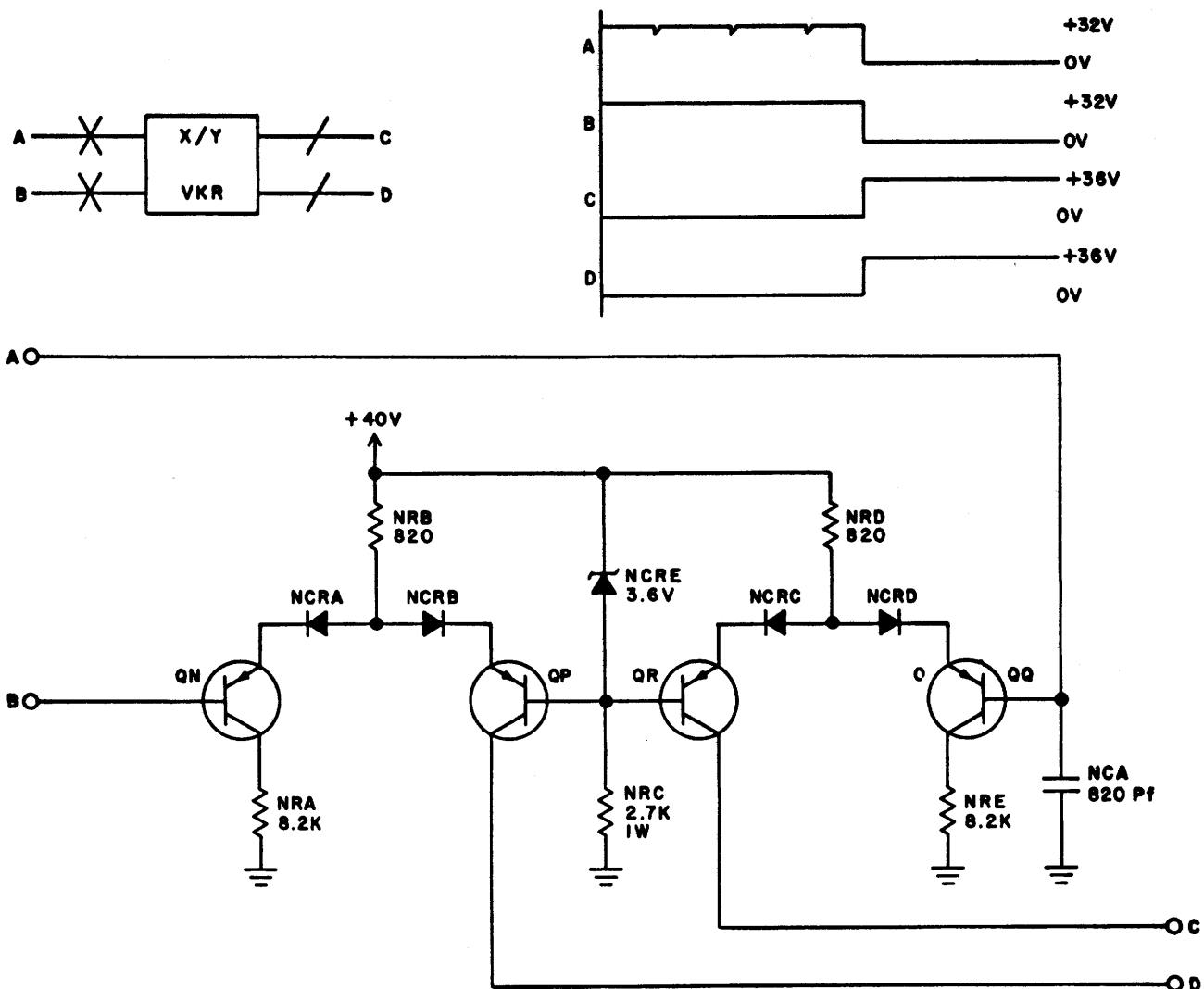


NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7K32

Figure 7-63.1. Level Translator - VKP

Level Translator - VKP

The VKP circuit connects input A to the writer side of the DC Current Detector (VKR). It converts the non-standard input level to a standard TTL level at output C.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7K31

Figure 7-63.2. DC Current Detector - VKR

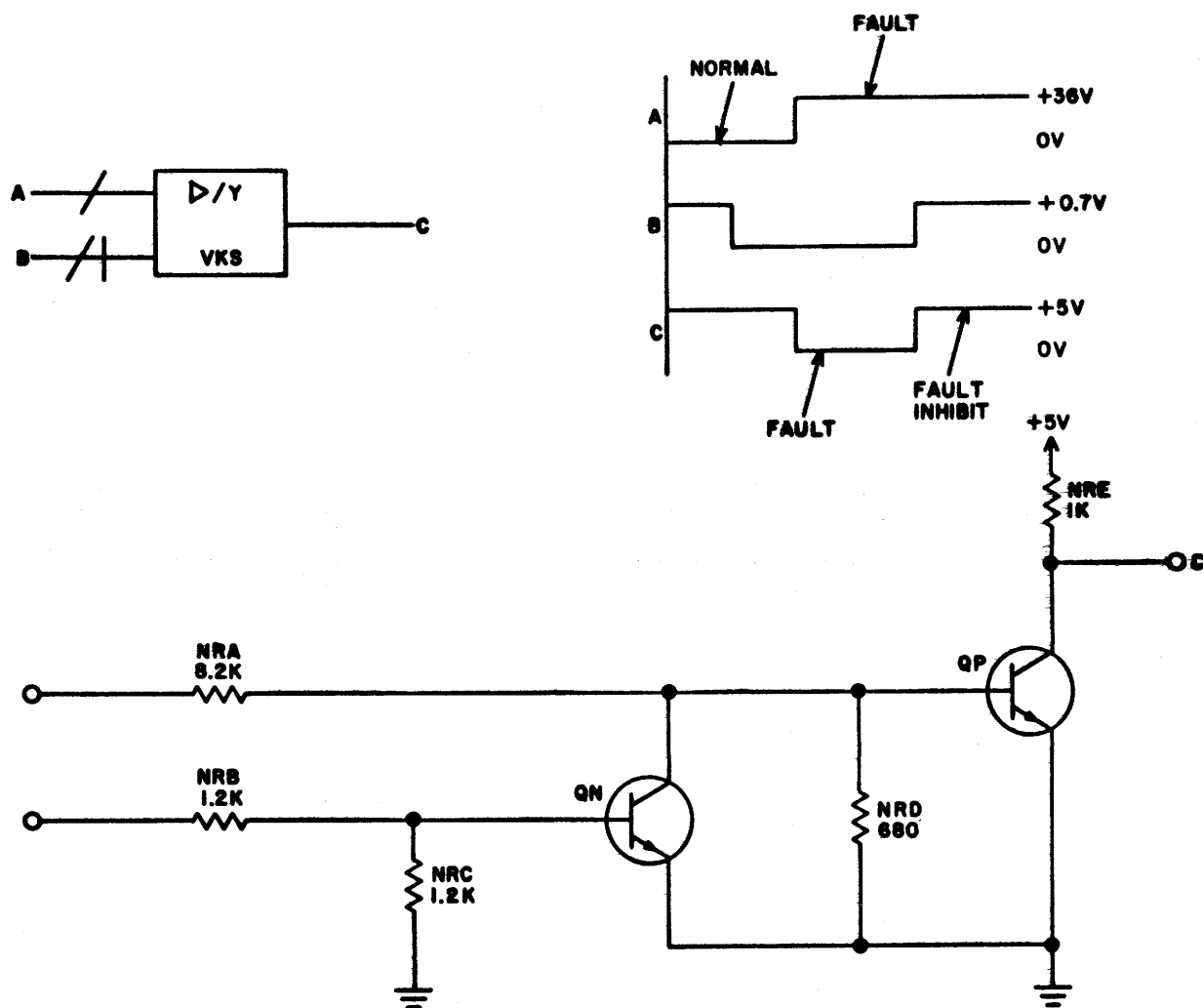
DC Current Detector - VKR

The VKR circuit is made up of two comparator stages. The write current detection stage consists of transistors QR and QQ, resistors NRD and NRE, diodes NCRC and NCRD, and capacitor NCA. The erase current detection stage consists of transistors QN and QP, resistors NRA and NRB, and diodes NCRA and NCRB. A reference voltage for both stages is provided by zener diode NCRE and resistor NRC.

Input A comes from the write driver circuit where the two driver transistor collectors are common. With the write driver circuit operating properly, input A is less positive than the reference voltage, QQ is on, and QR is off. Hence output C is at 0 vdc.

As the write current drops, input A becomes more positive until QQ is turned off. This turning QR on, causing output C to go to +36 vdc. Capacitor NCA filters out switching transients.

Input B comes from the erase driver circuit. Output D is used for this comparator stage. Operation of the erase comparator is identical to the write comparator.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

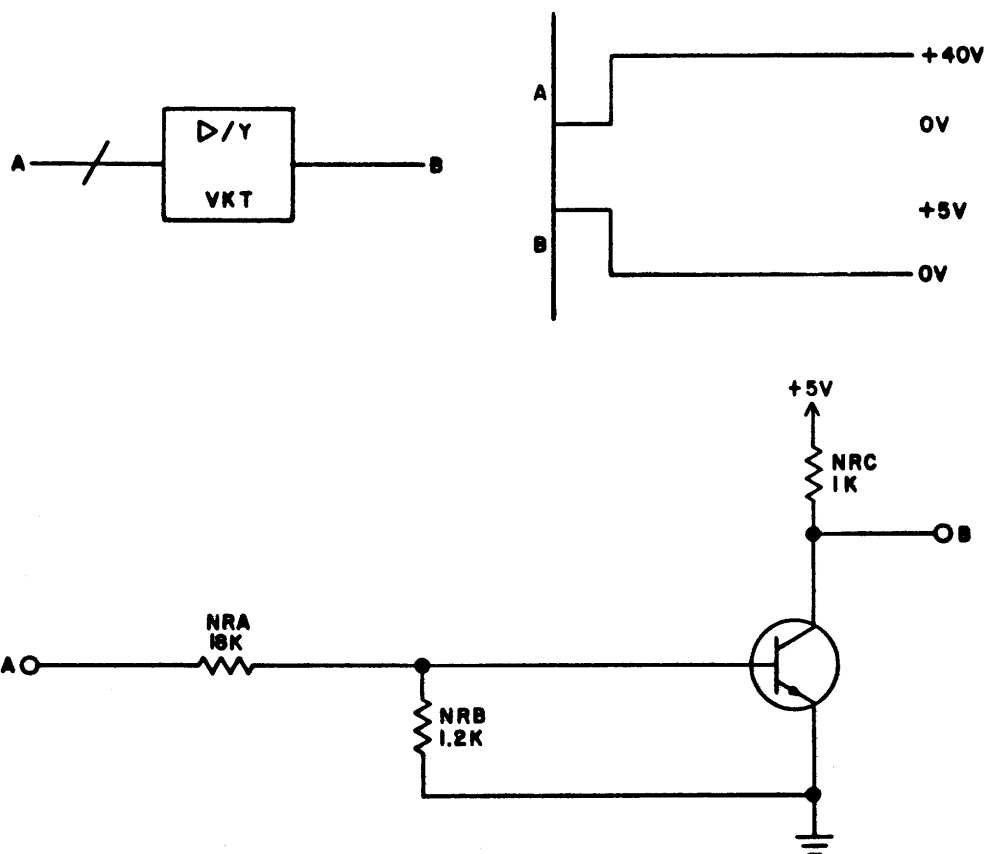
7K33

Figure 7-63.3. Gated Level Translator - VKS

Gated Level Translator - VKS

The VKS circuit connects input A to the erase side of the DC Current Detector (VKR). It converts the non-standard input level to a standard TTL level.

Transistor QN and resistors NRB and NRC form an inhibit gate. A fault indication is passed on when input B is 0 vdc, and inhibited when input B is +0.7 vdc.

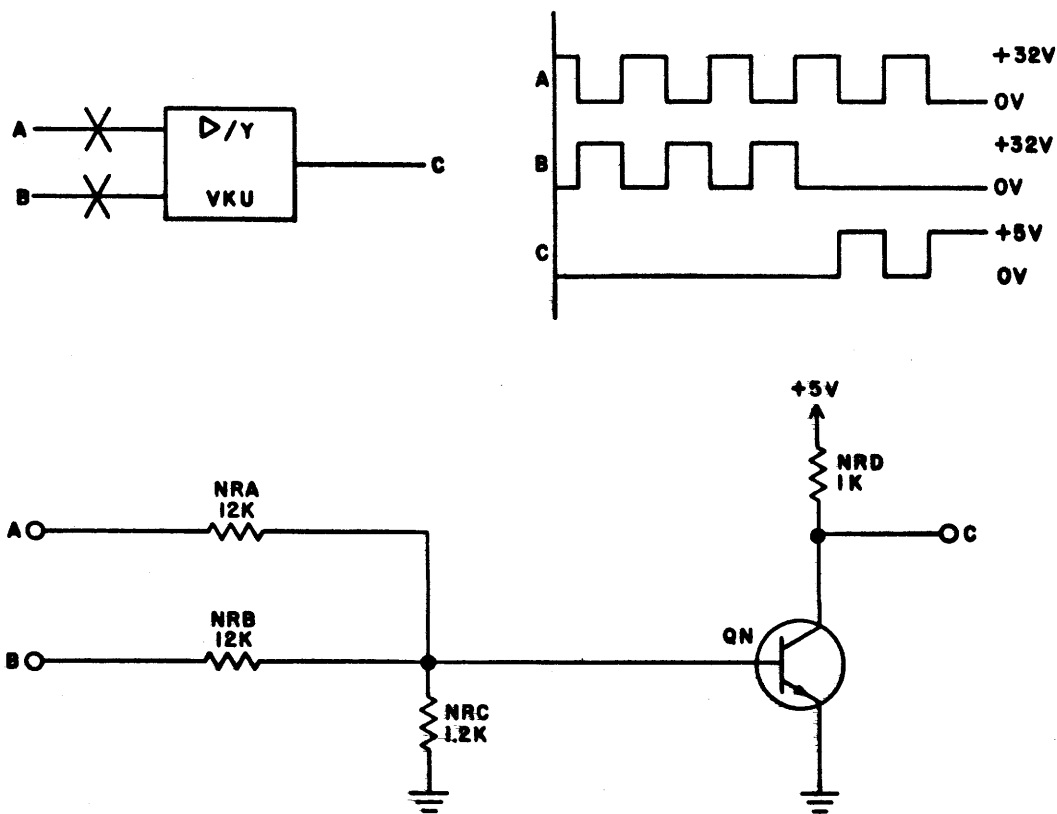


NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7K34

Figure 7-63.4. Erase Cutoff Detector - VKT

Erase Cutoff Detector - VKT

The VKT circuit converts a non-standard input A to a standard TTL level at output B. When the erase circuit is on, input A is +40 vdc, QN is on, and output B is 0 vdc. When erase is off, input A is 0 vdc, QN is off and output B is +5 vdc.

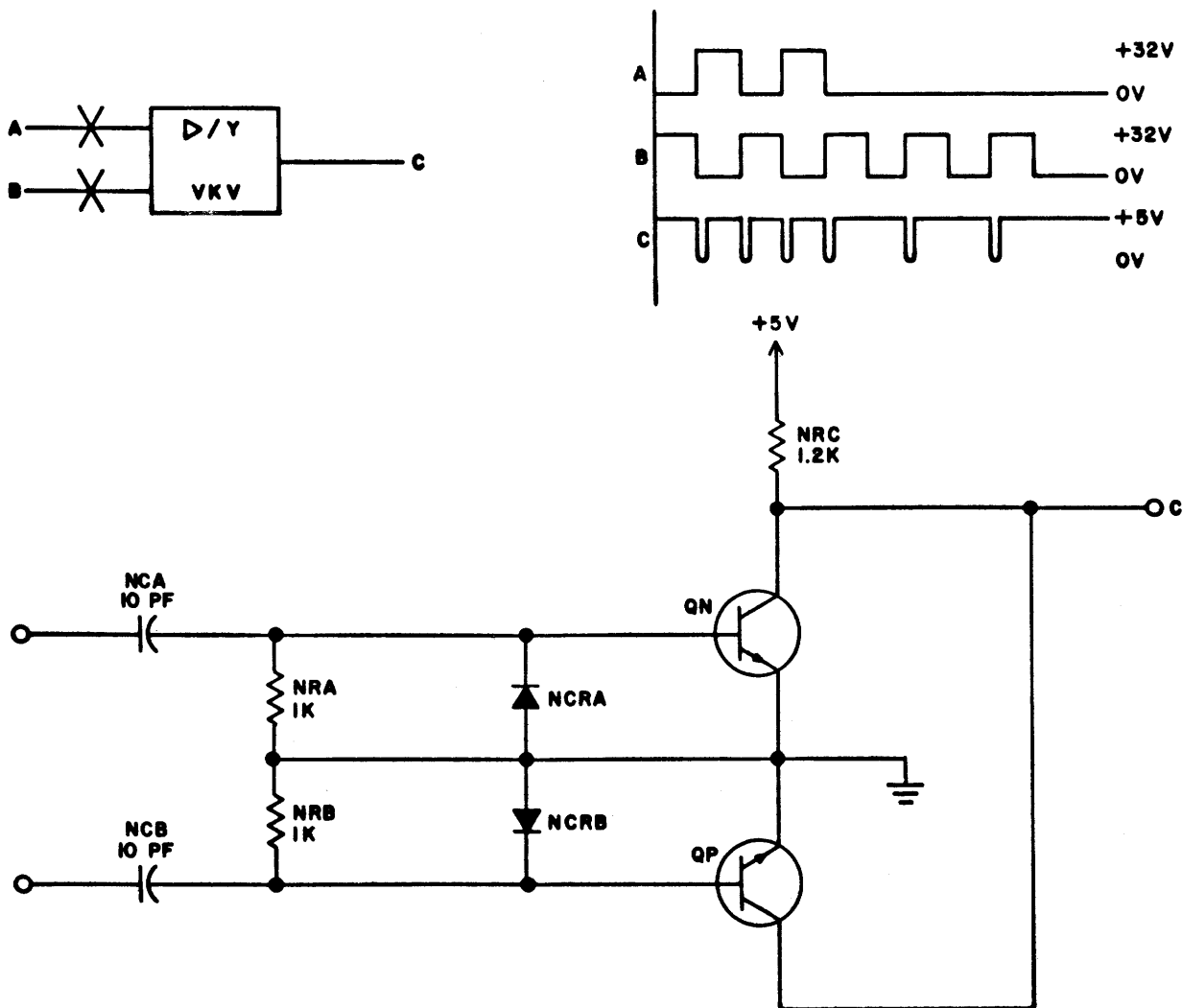


NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7K27

Figure 7-63.5. Write Shutoff Detector - VKU

Write Shutoff Detector - VKU

The VKU circuit is an "or" function that outputs 0v under normal write operations. Inputs A and B come from the output of the Write Driver. A voltage present on either A or B turns QN on. If only half of the write driver is functioning, output C toggles. If neither side of the write driver is functioning, output C is a static "1".



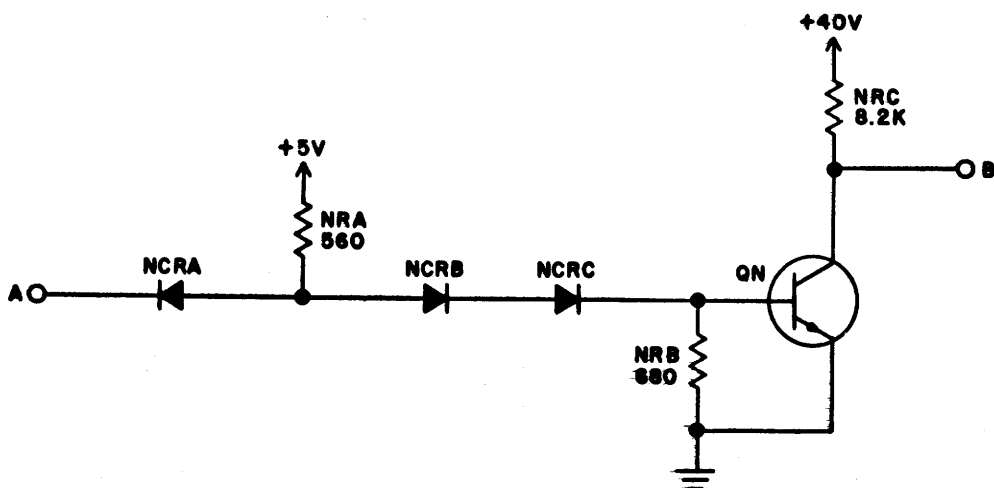
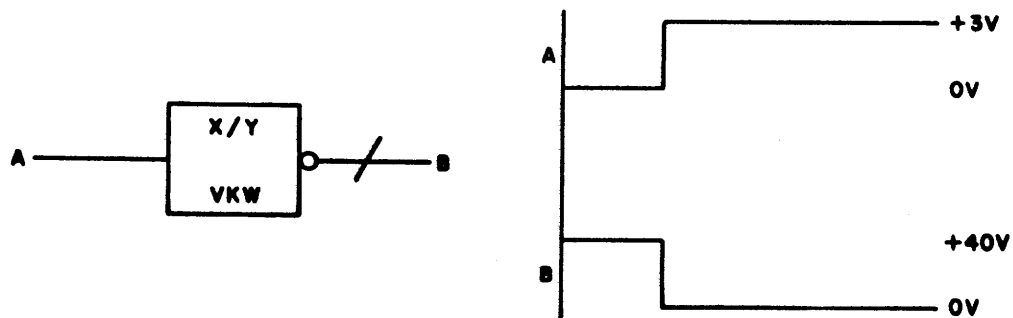
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7K28

Figure 7-63.6. AC Write Current Detector - VKV

AC Write Current Detector - VKV

The VKV circuit outputs a negative-going pulse for each positive transition of the write driver. When input A goes positive, NCA charges, turning QN on. This causes output C to go 0v. When NCA is fully charged, QN is turned off and output C goes back to +5v. QP works in the same manner. Diodes NCRA and NCRB limit the negative transitions at the base of QN and QP to 0.7v. When write is off, output C is a "1".



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7K26

Figure 7-63.7. Level Translator - VKW

Level Translator - VKW

The VKW circuit converts a logic "0" to a +40v (nominal) level used in the write circuitry. When a logic "1" is present at input A, transistor QN saturates and the output goes to 0v.

Flip-Flop-WBB

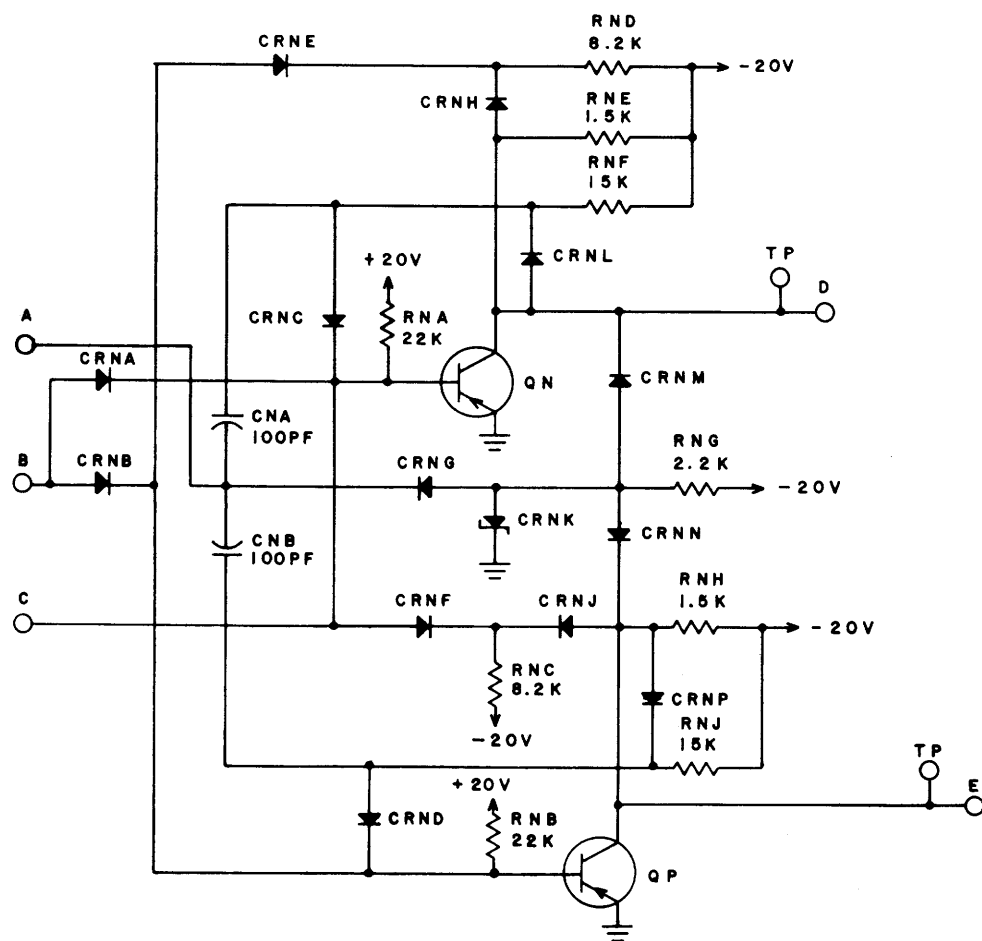
The WBB circuit (Figure 7-64) is a toggle flip-flop with gate and data inputs.

Input B holds both transistors off by grounding the bases when the circuit is off. When a write operation is to be performed, the base of QP is released while QN is still grounded by input C. This sets an initial condition for the flip-flop: QP is on, QN is off.

After the flip-flop is pre-set, it is toggled through input A by a series of negative data pulses. The leading edge of the negative data pulse begins charging capacitor CNB. Diode CRND becomes forward biased. QP is on. Output E is at ground. A voltage of -3.6v across Zener diode CRNK keeps CRNN reverse biased. CRNK and CRNM clamp the output of QN at -3.8v.

The trailing edge of the data pulse results in a positive pulse to the base of QP. Transistor QP turns off. Output E goes toward -4v. Both sides of CNA are at ground. Therefore, CRNC and CRNF are forward biased by the -20v source through RNC. The base of QN goes negative. Transistor QN turns on and output D drops to ground. Diodes CRNM and CRNJ are now reverse biased. Since the collector of QP is more negative than the voltage across Zener diode CRNK (-3.6v), CRNN is forward biased. This clamps the voltage at output E at approximately -3.8v.

The leading edge of the next negative pulse charges CNA and discharges CNB since both sides of CNB are at about -3.8v. The flip-flop will toggle on the ground-going edge of the pulse in the same manner as described for the first pulse.



6T127

7-91

Toggle Flip-Flop - WBC

Inputs to A and B of the WBC flip-flop (Figure 7-65) are either a positive pulse or ground. If A has positive pulse, then B is at ground. If A is at ground then B has a positive pulse. If input A receives a positive pulse, output C will be at ground and output D will be a constant positive voltage. A positive pulse at B will toggle the flip-flop. C will then be a positive voltage and D will be at ground.

A positive pulse to input A turns on transistor QN, which drives the base of QR to ground. Transistor QR is turned off. Input B is at ground and QP is off. The base of QQ is, therefore, positive and QQ turns on. This latches the base of QR at ground and puts a ground on output C. With QP off and QR latched off, current flows from the +20v source through RNB to output D.

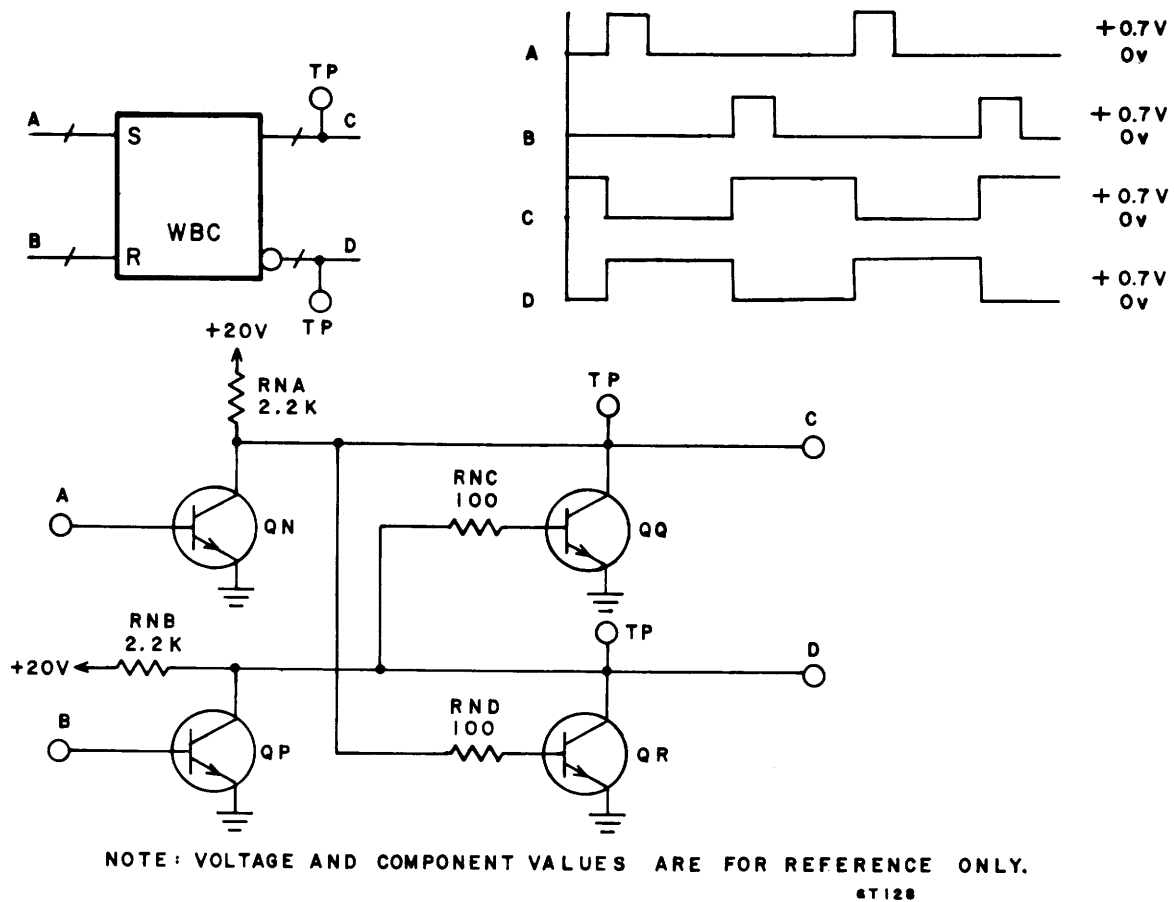


Figure 7-65. Toggle Flip-Flop - WBC

When a positive pulse is felt at B, QP turns on. This drives the base of QQ to ground, turning QQ off. Input A is at ground and QN is off. The base of QR is, therefore, positive. Transistor QR conducts, latching the base of QQ at ground and driving output D to ground. With QN and QQ off, output C is positive.

Single Shot - XAA

The input to A and B (Figure 7-66) of the XAA circuit is a 0.7v balanced square wave centered around a positive voltage. Each time the inputs change polarity a short negative pulse is formed at output C.

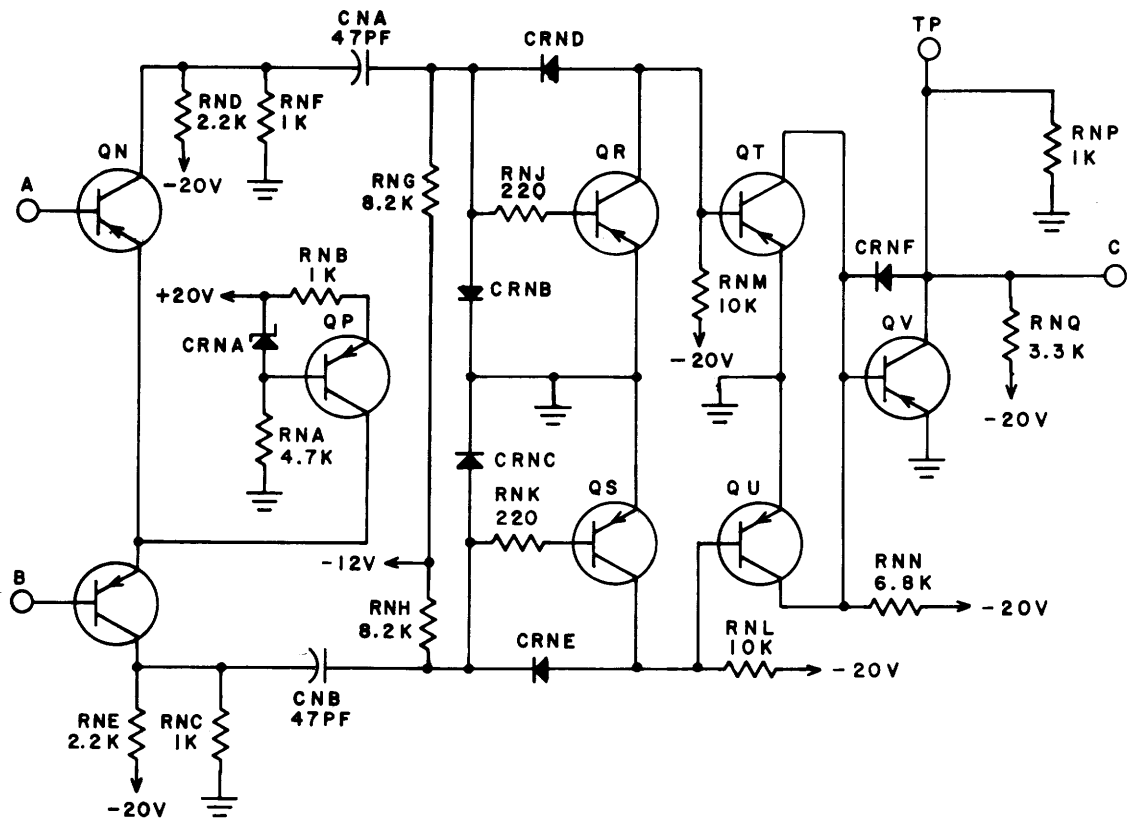
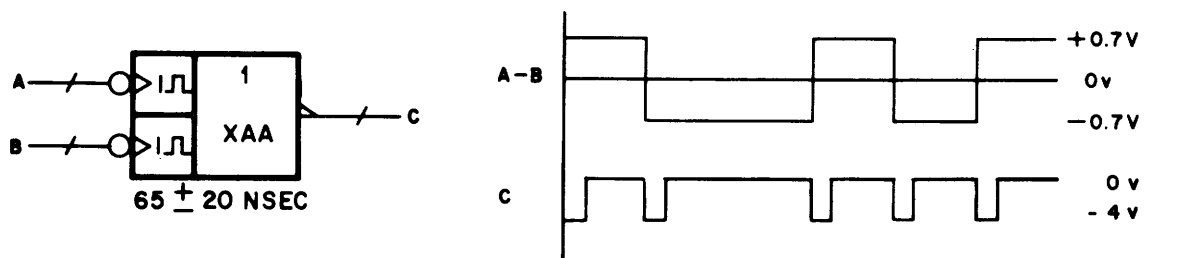
The square wave input is sufficient to alternately turn QN and QQ on and off. A current of about 5.6 ma is alternately switched between QN and QQ. When input A is more positive than input B, QN turns off. The voltage at the collector of QN is about -20v. The voltage at the junction of RNG and RNJ is -1.6v. When the inputs switch, QN turns on. The collector of QN rises to about -8.7v. CNA forms a positive pulse to the base of QR. The positive pulse turns QR off, QT on and QV off for the duration of the pulse. The amplitude of the pulse is limited by CRNB. Charging time for CNA is about 100 nsec. When the inputs switch again, QQ turns on and QN turns off. CNB forms a positive pulse which turns QV off again for the duration of the pulse. The output at C is ground until QV is turned off. During the short time that QV is off, a negative pulse appears at output C.

Diodes CRND and CRNE prevent saturation of QR and QS. As the collectors of QR and QS approach ground, the negative voltage at the left ends of RNJ and RNK is limited to the sum of the voltage drops across QR and CRND or QS and CRNE, respectively. Diode CRNF prevents QV from saturating.

Single Shot - XAB

The input at A of the XAB circuit (Figure 7-67) is a balanced square wave between 0v and +0.75v. The output at B is normally positive, but drops to ground for a short time at the leading edge of the ground portion of the input wave.

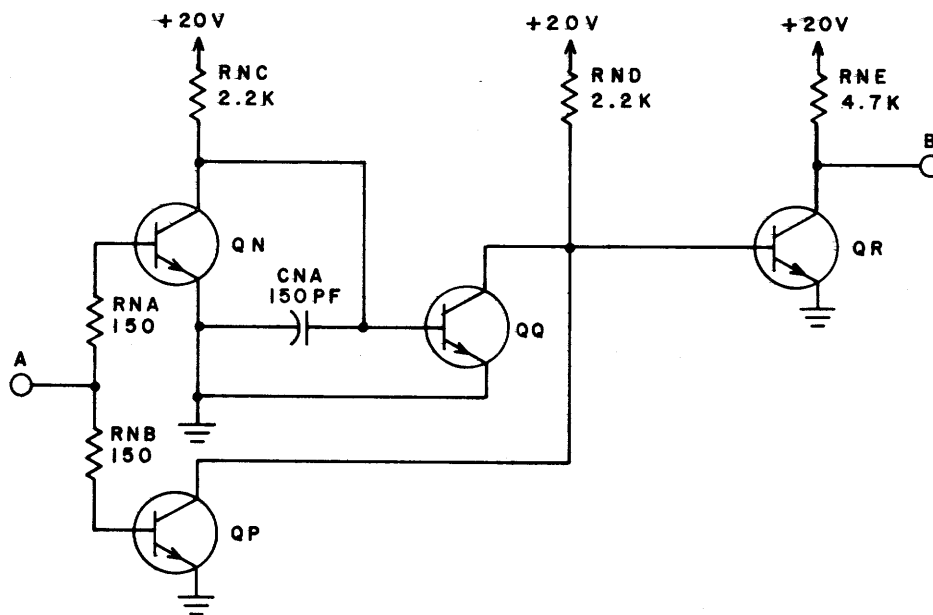
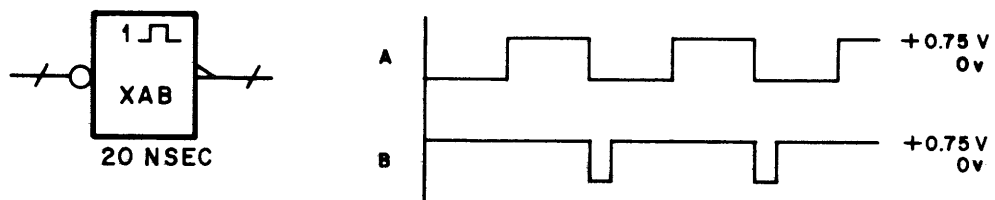
During the positive portion of the input wave, transistors QN and QP are on. This leaves the bases of QQ and QR near ground. Transistors QQ and QR are off. The output at B is a positive voltage supplied through resistor RNE.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

6T129

Figure 7-66. Single Shot - XAA



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

6T130

Figure 7-67. Single Shot - XAB

When the input wave goes to ground, transistors QN and QP turn off. With QP off, the base-emitter junction of QR is forward biased. Transistor QR conducts and the output at B drops to near ground. With QN off, capacitor CNA charges toward +20v. When the charge on CNA reaches a level sufficient to turn on QQ, the base of QR again drops to ground. Transistor QR turns off. The output at B returns to the positive level.

Gated Single Shot - XAC

The XAC circuit (Figure 7-68) produces a 100-nsec ground pulse at output C when the inputs at A and B change state. The output is normally positive. Input A is connected to the set side of a flip-flop and input B is connected to the clear side.

When the flip-flop is clear, the base of QR is positive. Transistor QR conducts 10 ma of current from the -20v supply through RND, RNC, QS, QR and RNB. The collector of QN is at +20v and the collector of QR is near +13v. Transistors QT and QU are on and QV and QW are off.

When the flip-flop sets, QR turns off and QN turns on. The collector of QN goes to +13v, which drives the base of QT to about -6v. This turns QT off, driving the base of QV positive. QV turns on and the output at C goes to ground. Capacitor CNA charges through RNE with a time constant of 135 nsec. After 100 nsec the voltage at the base of QT has risen to +0.7v and QT turns on. This drives the base of QV to ground. QV turns off and the output at C returns to a positive level.

When the flip-flop clears again, a 100-nsec ground pulse is formed at C by QR, CNB, QU and QW.

Single Shot - XAE

The XAE circuit (Figure 7-69) is a combination inverter and pulse shaper. The circuit monitors the voltage fluctuations across the head write coils. Its output is used to detect the occurrence of a fault during a write operation.

Inputs A and B are connected across the center-tapped (to ground) pair of write coils. As write current changes polarity, a negative pulse from the undriven coil momentarily turns on QN. When QN turns on, capacitor NC1 discharges through the base of QP. Transistor QP is already on, so the discharge causes it to draw more current. As the write current polarity changes, QN turns off and NC1 charges to -5 volts via diode NCR1 and resistor NR2. This action momentarily provides reverse bias to QP and turns it off for 50 nanoseconds to

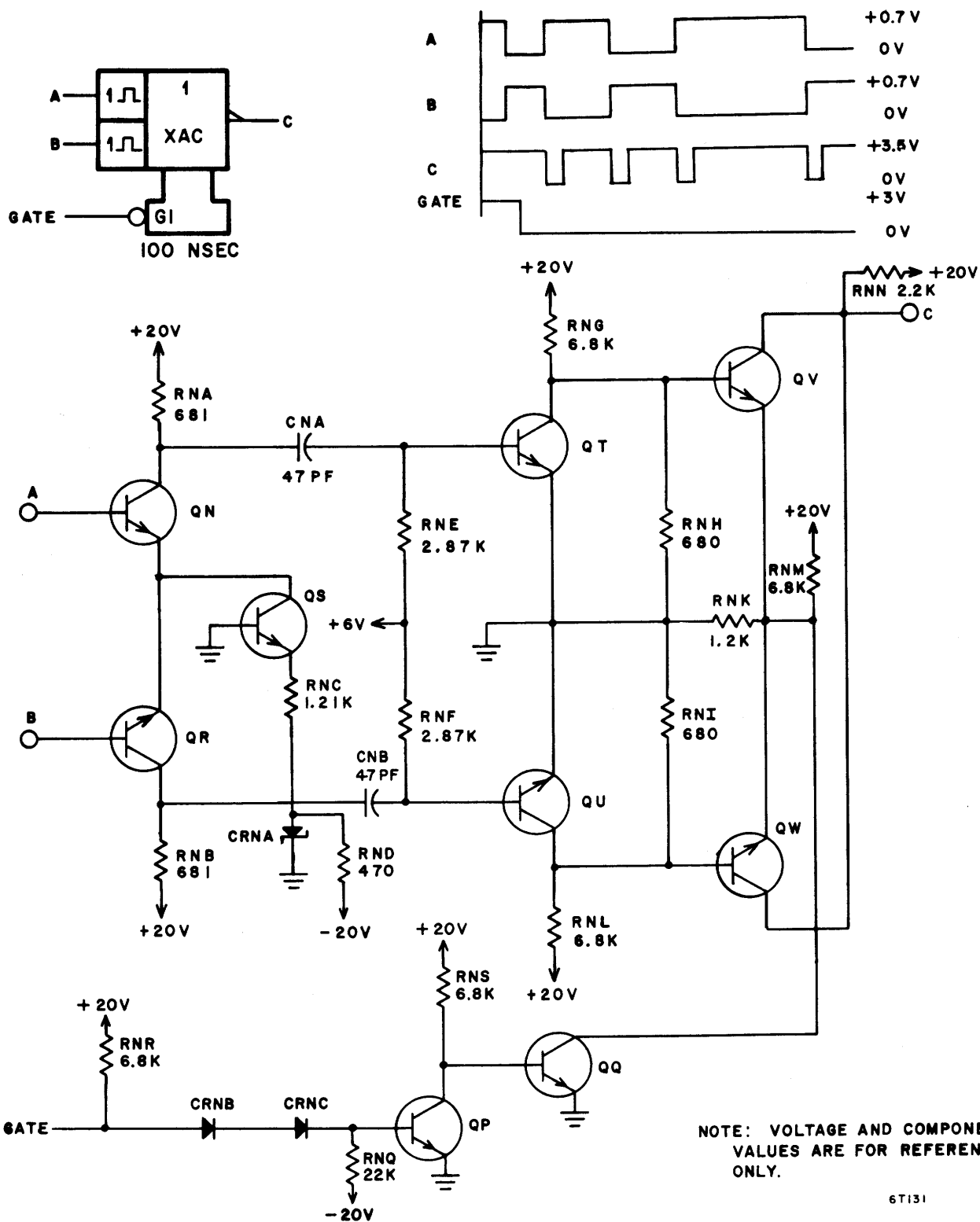
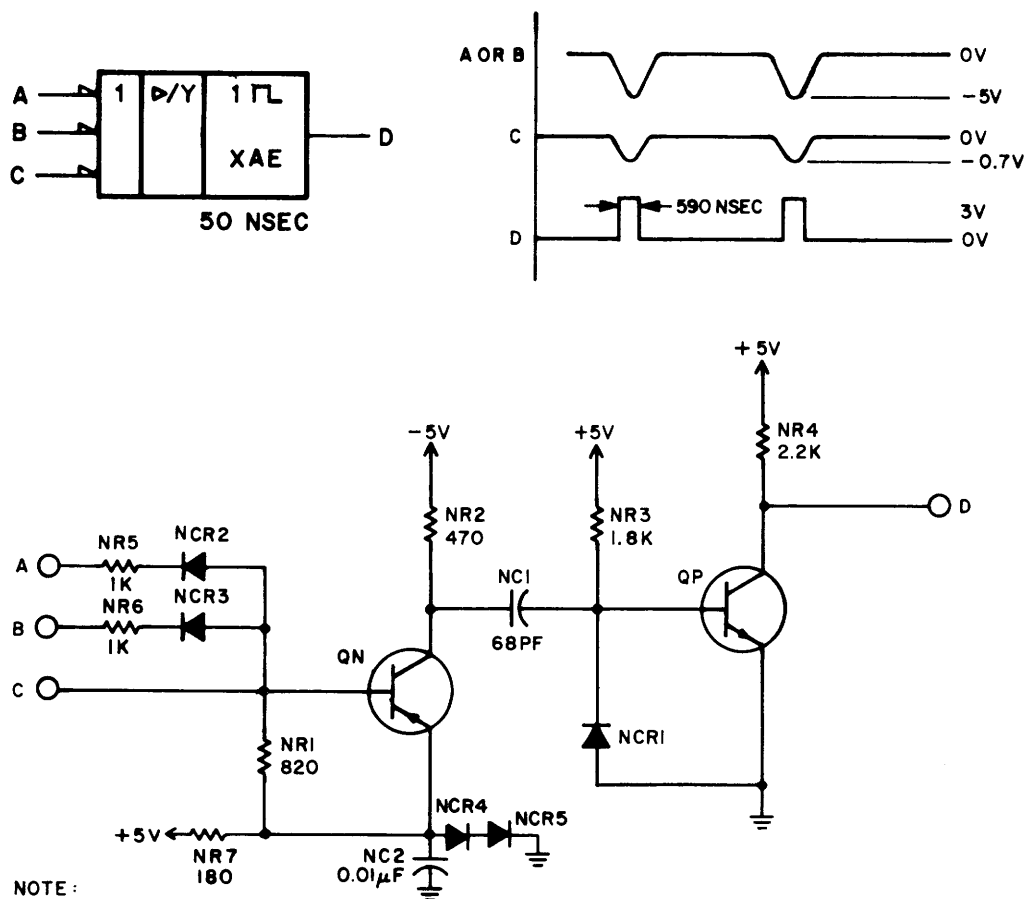


Figure 7-68. Gated Single Shot - XAC

cause a positive pulse at output D. A pulse appears at D for each transition of the head write current. The pulses drive a single-shot IC circuit which, if allowed to time out, will signal a fault.



NOTE:

I. VOLTAGE AND COMPONENT VALUES FOR REFERENCE ONLY

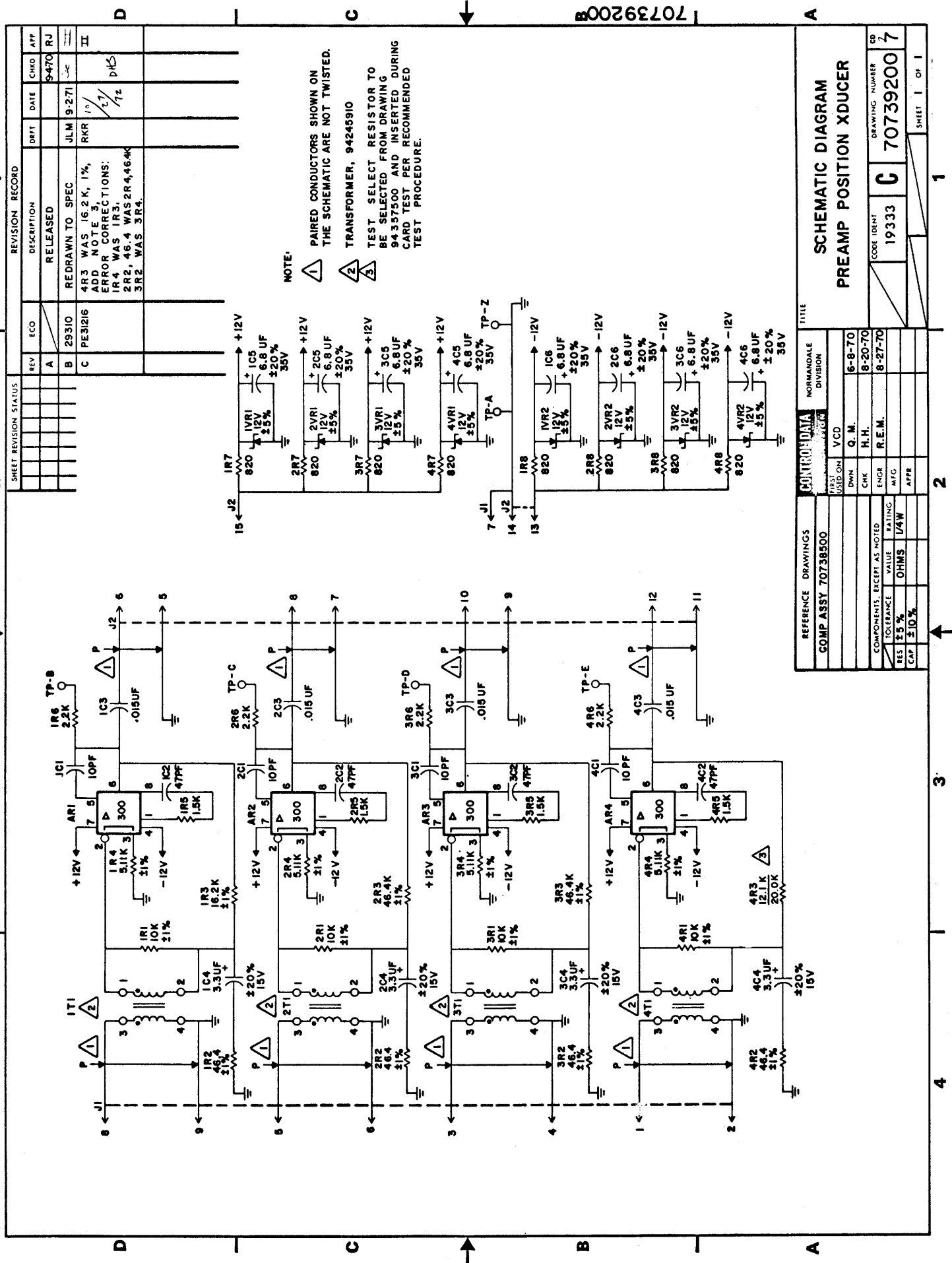
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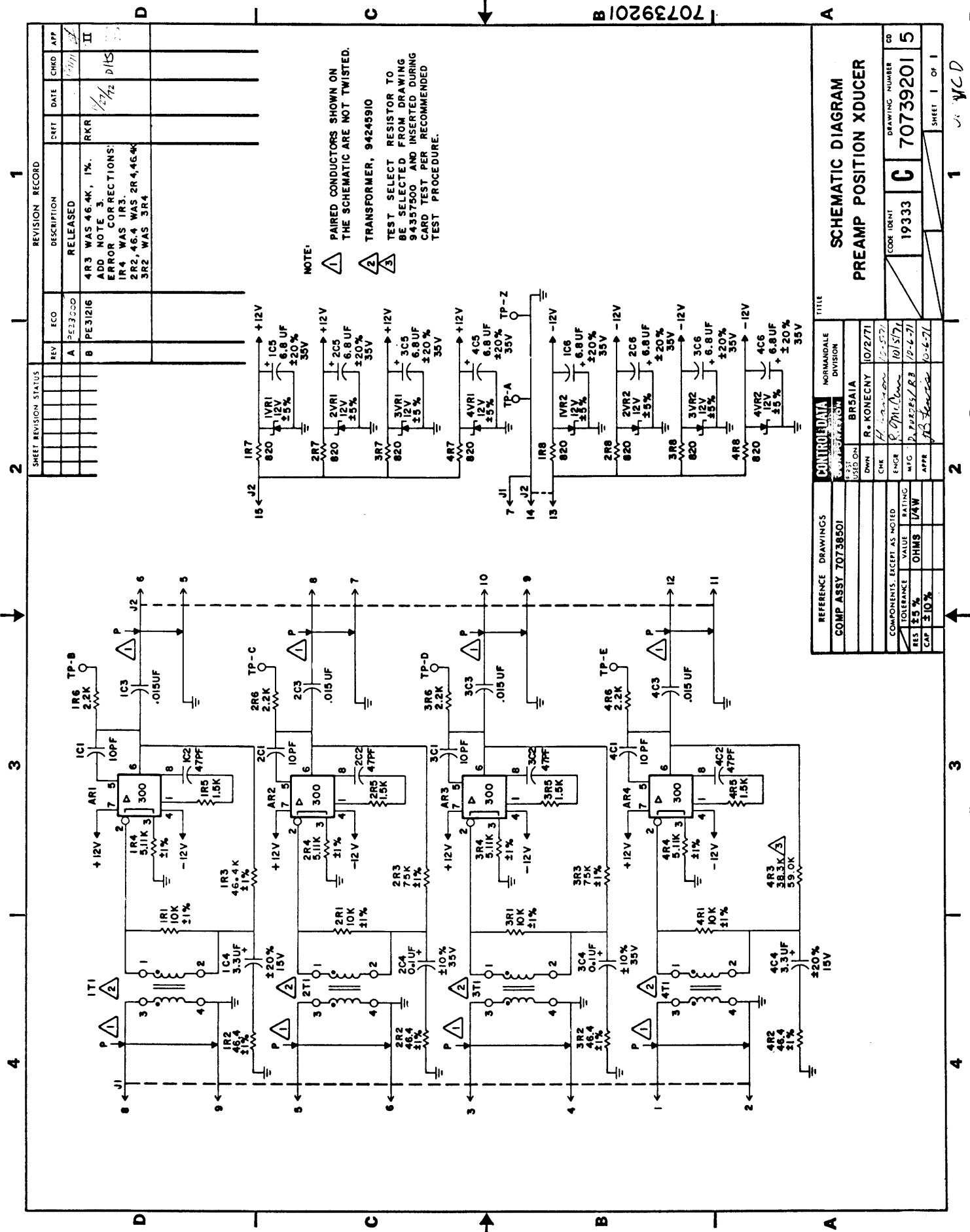
Figure 7-69. Single Shot - XAE

PART 2

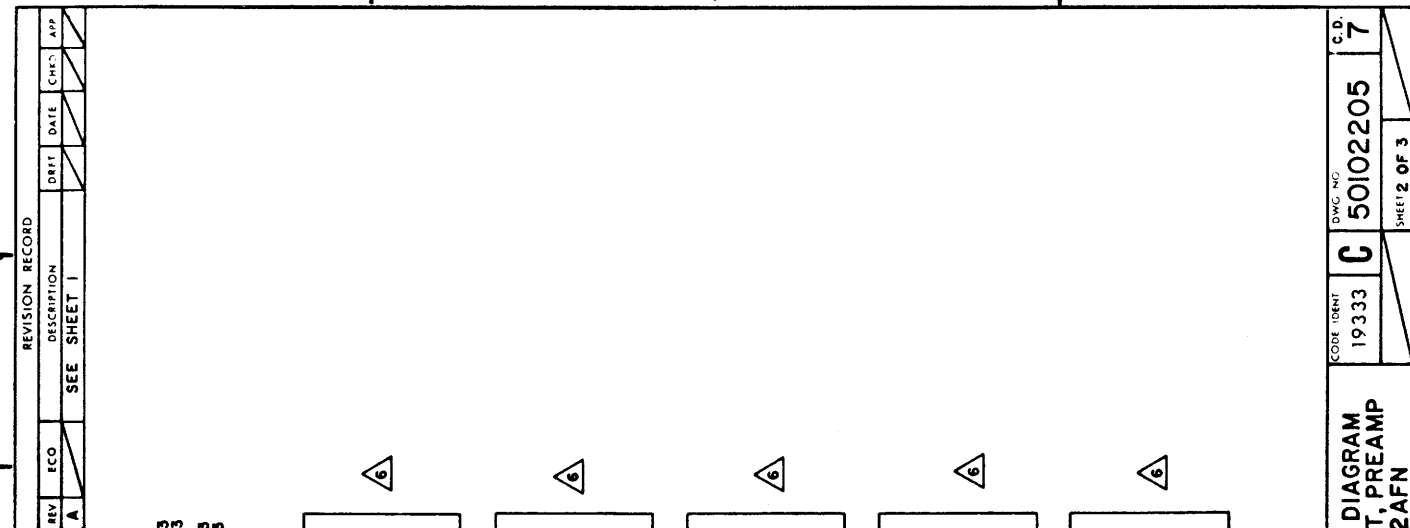
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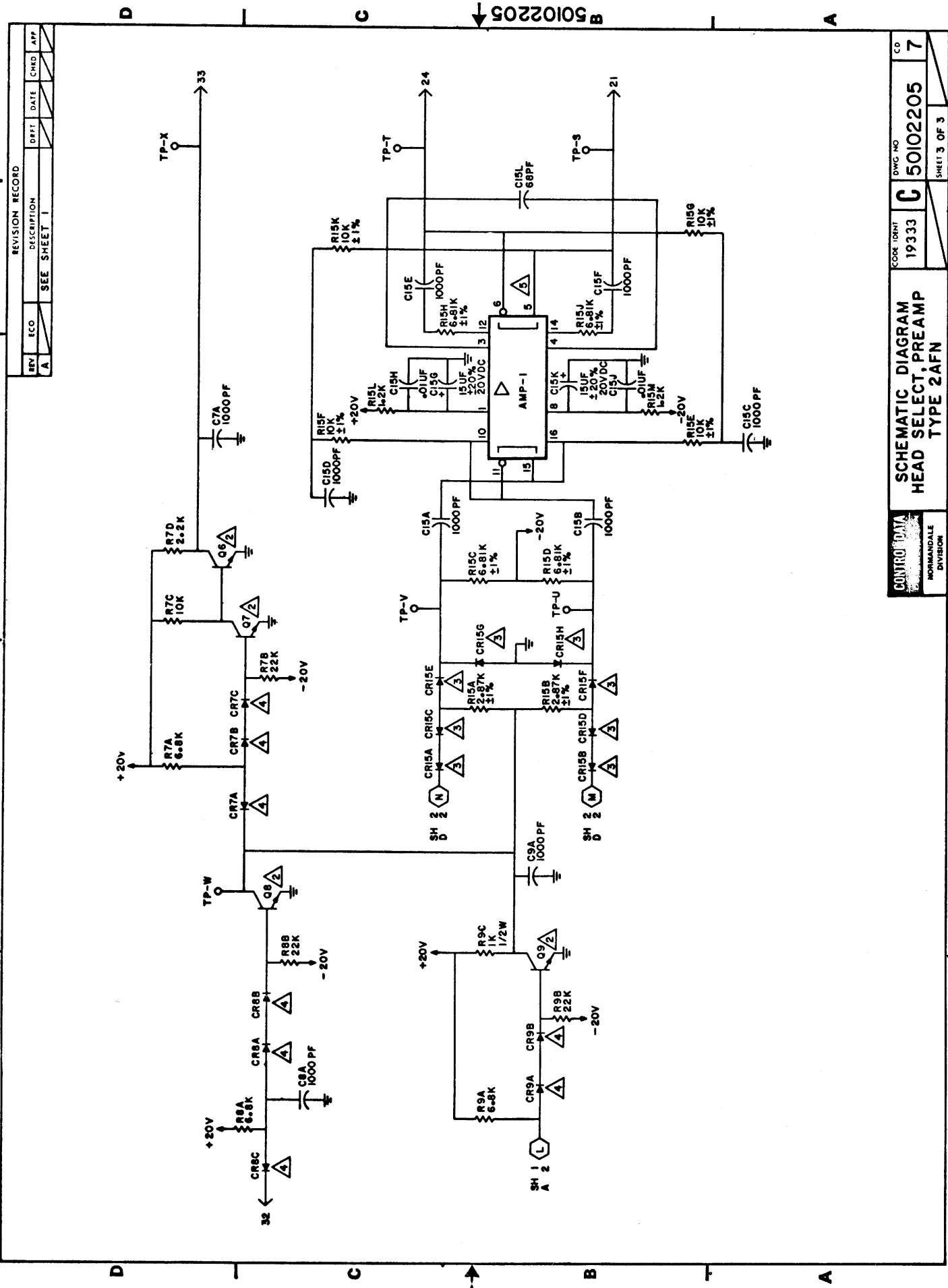




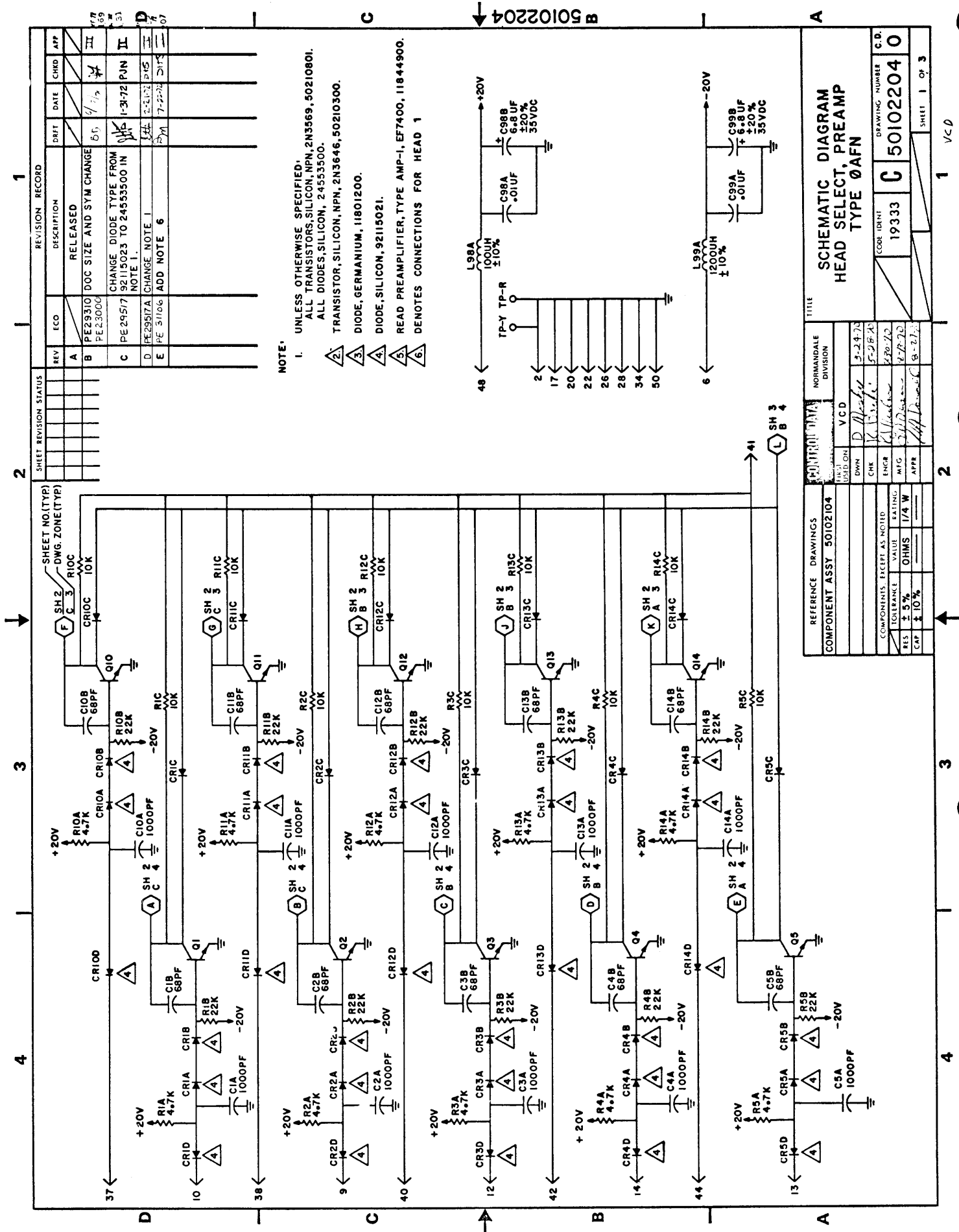








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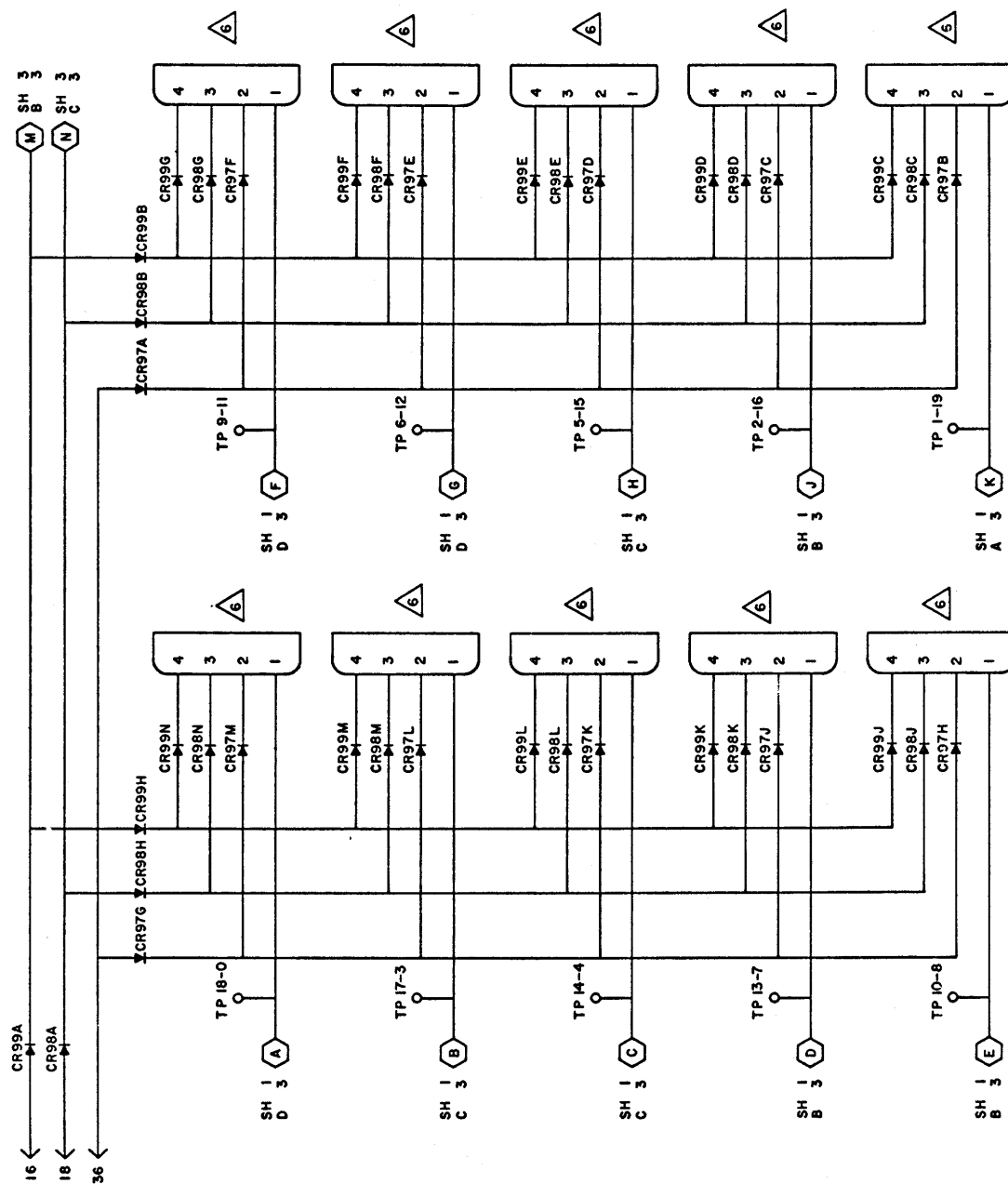
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- DIODE, GERMANIUM, 11801200.
- DIODE, SILICON, 92115021.
- READ PREAMPLIFIER, TYPE AMP-1, EF7400, 11844900.
- DENOTES CONNECTIONS FOR HEAD 1

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HEAD SELECT, PREAMP
TYPE ØAFN

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CAP ± 10%		APPR		8-21-72	
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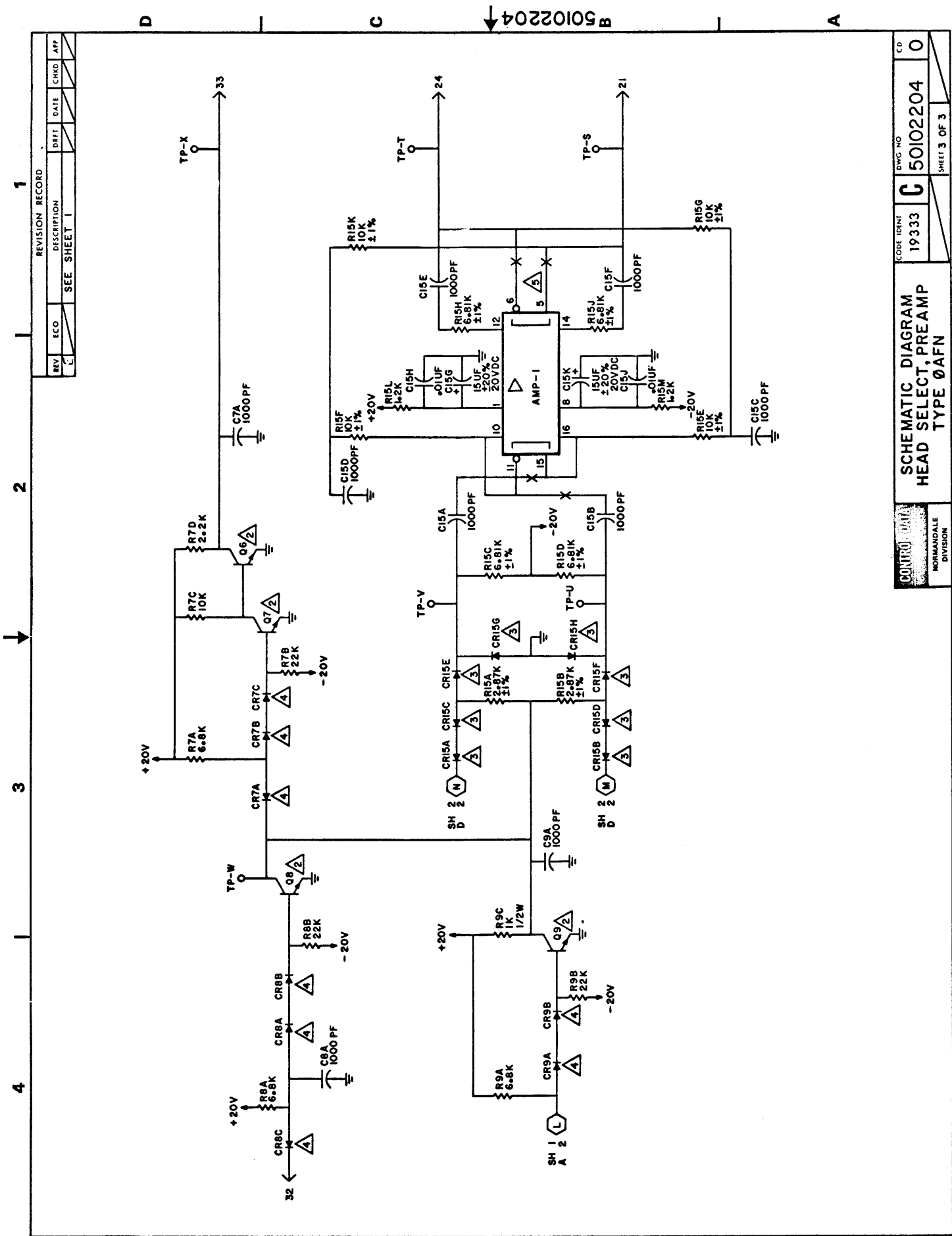


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TYPE ØAFN

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PAGE 2 OF 3

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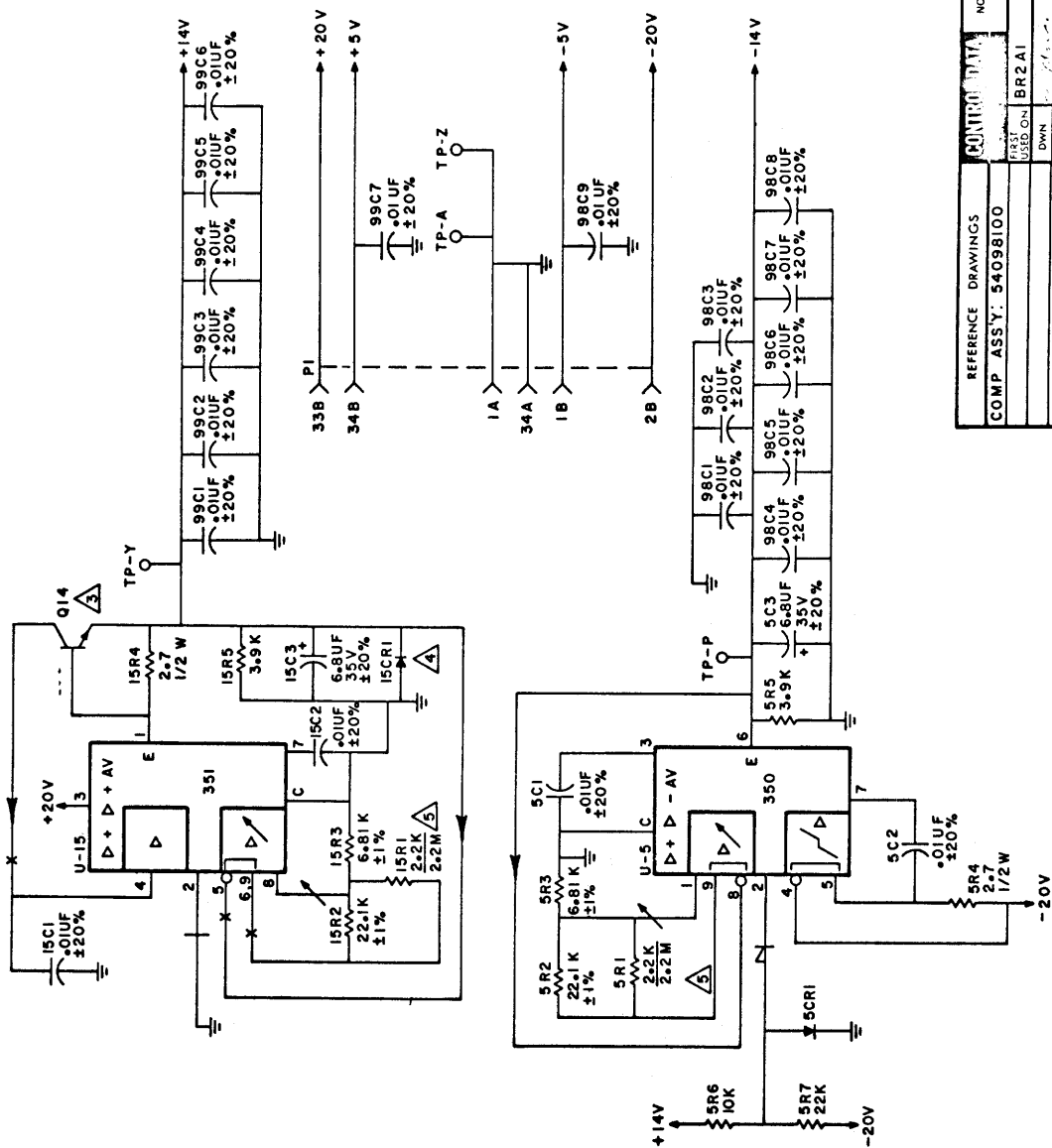


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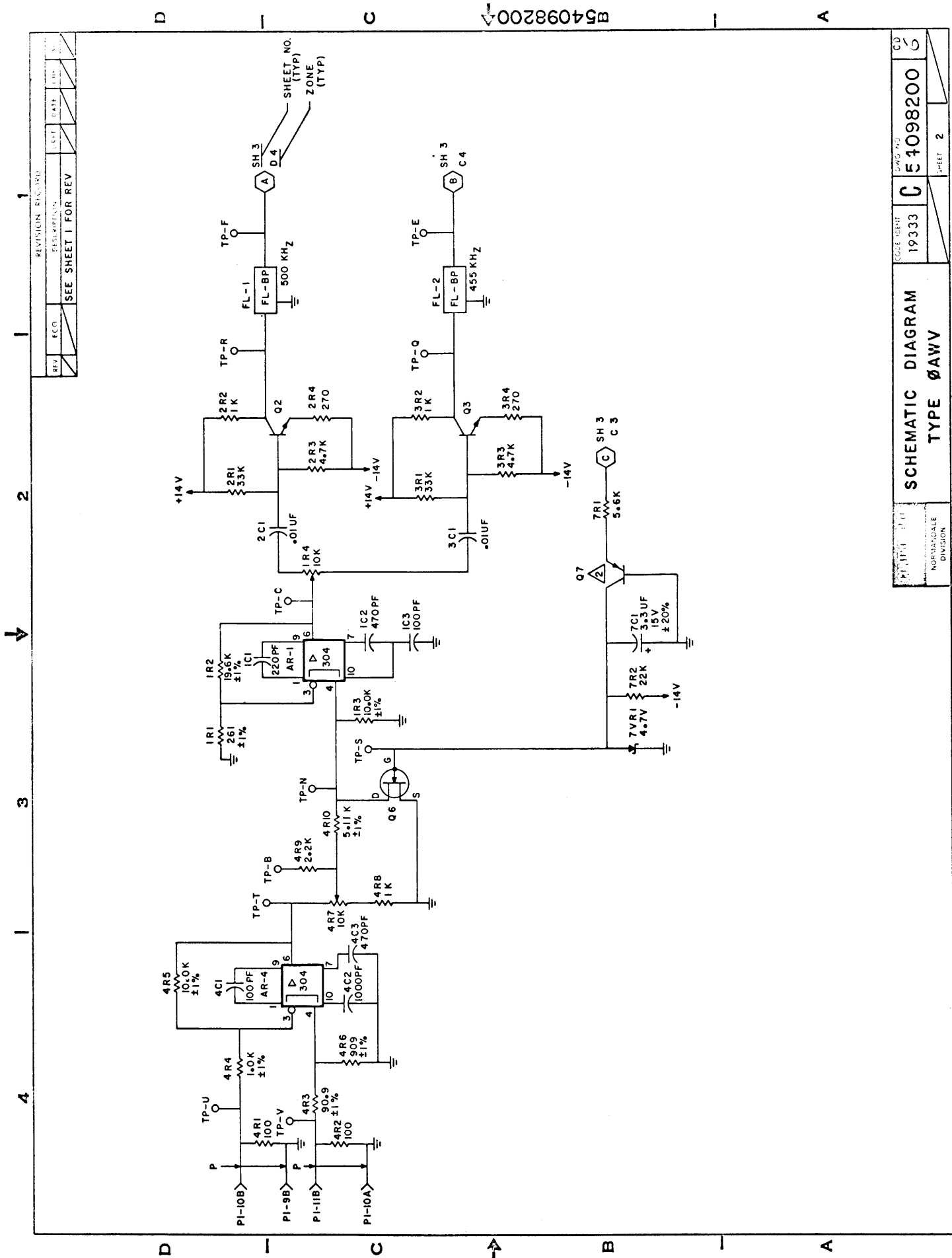
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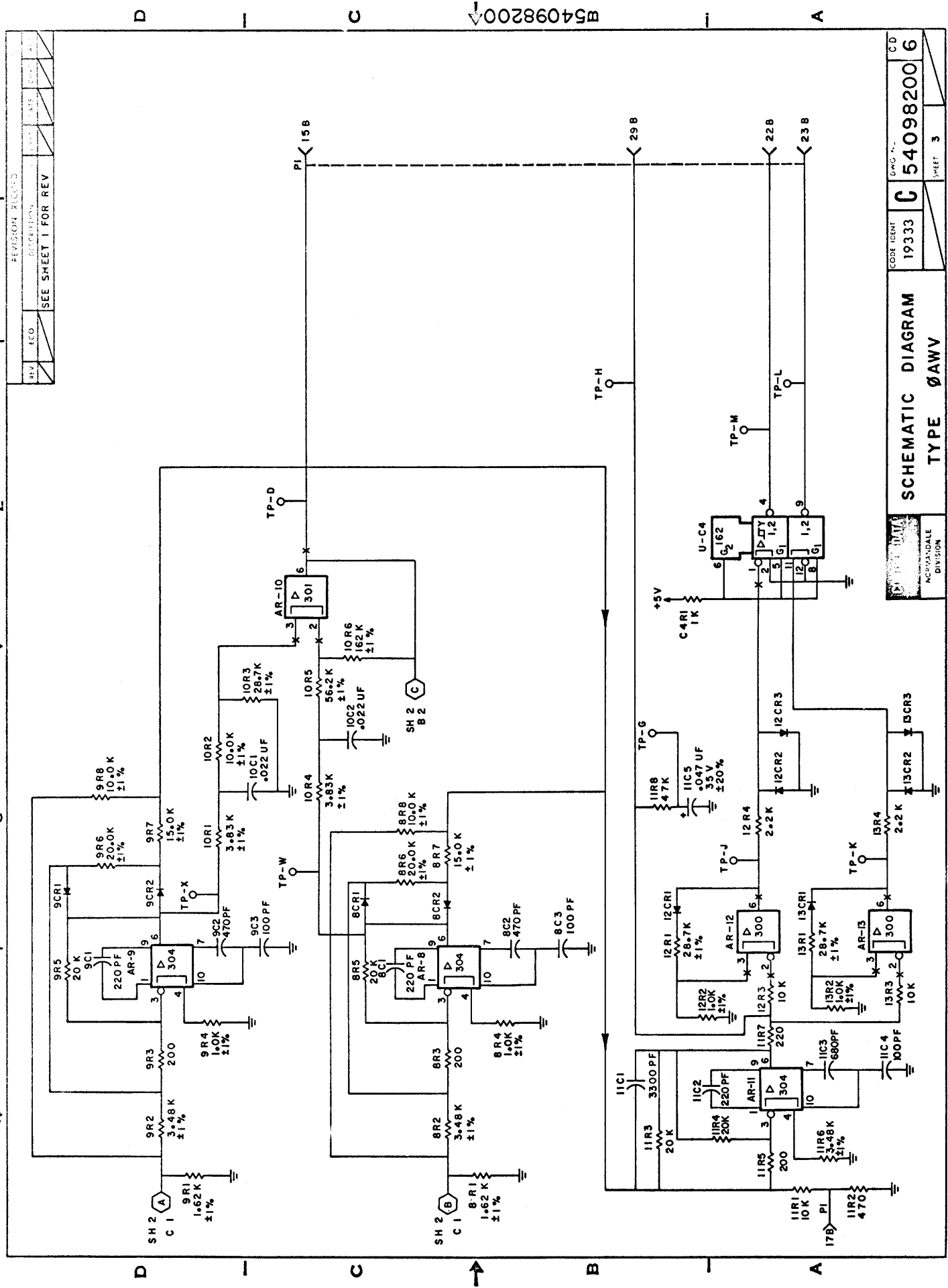
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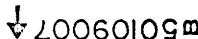
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ALL DIODES, SI, 92115023.
2. TRANSISTOR, SPNP, 2N4619, 50211610.
3. TRANSISTOR, SNPN, 2N3646, 50210310.
4. DIODE, GERMANIUM, 11801200
5. RESISTORS 5R1 AND 15R1 ARE SELECTED FROM 46325900.
6. ALL IC ELEMENT TYPE NO. 304 HAVE PINS 5 CONNECTED TO -14V AND PINS 8 CONNECTED TO +14V.
7. ALL IC ELEMENT TYPE NO. 300 AND 301 HAVE PINS 4 CONNECTED TO -14V AND PINS 7 CONNECTED TO +14V
8. IC 162 HAS PIN 7 CONNECTED TO GND, PIN 13 CONNECTED TO -5V AND PIN 14 CONNECTED TO +5V

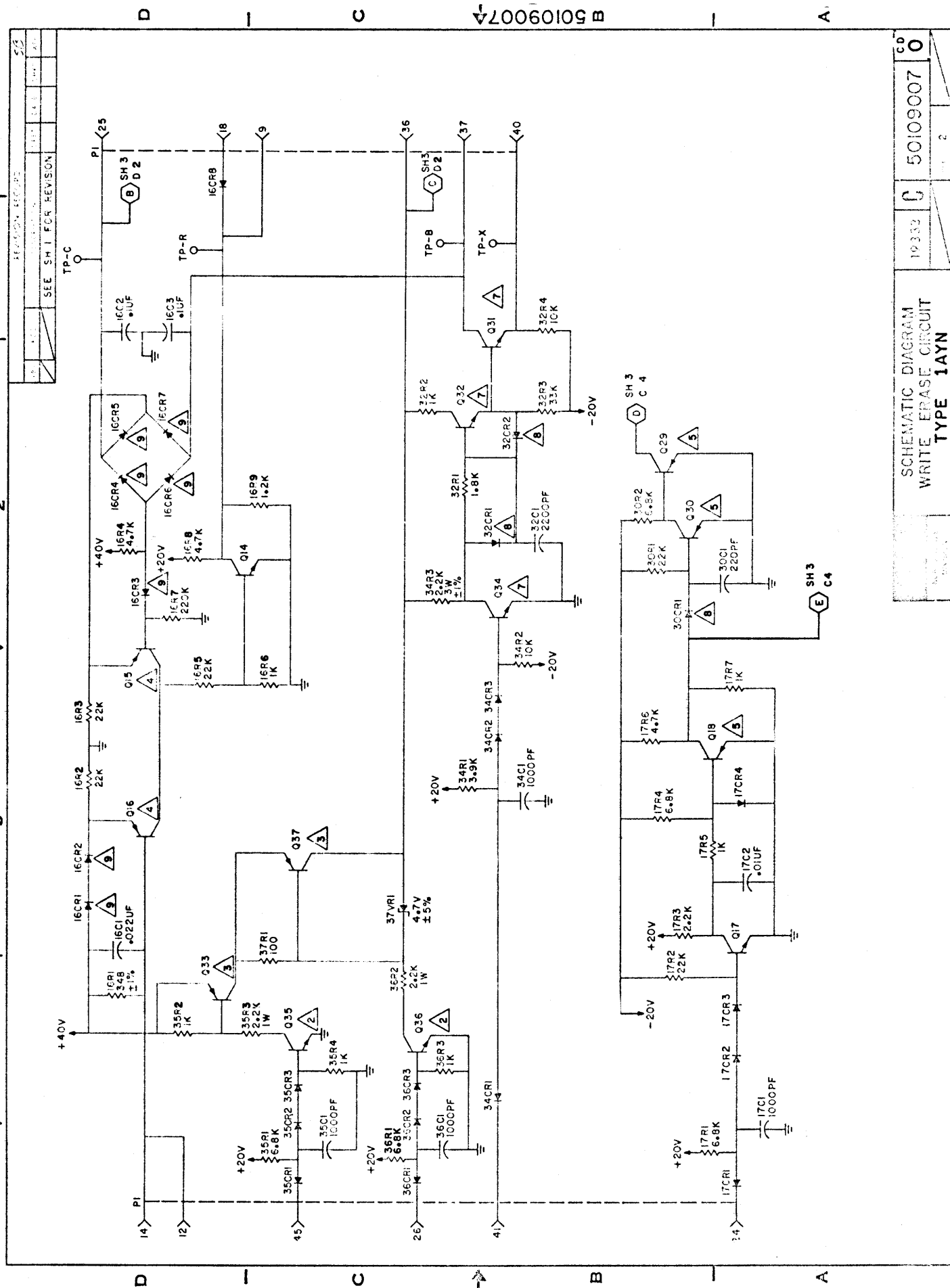


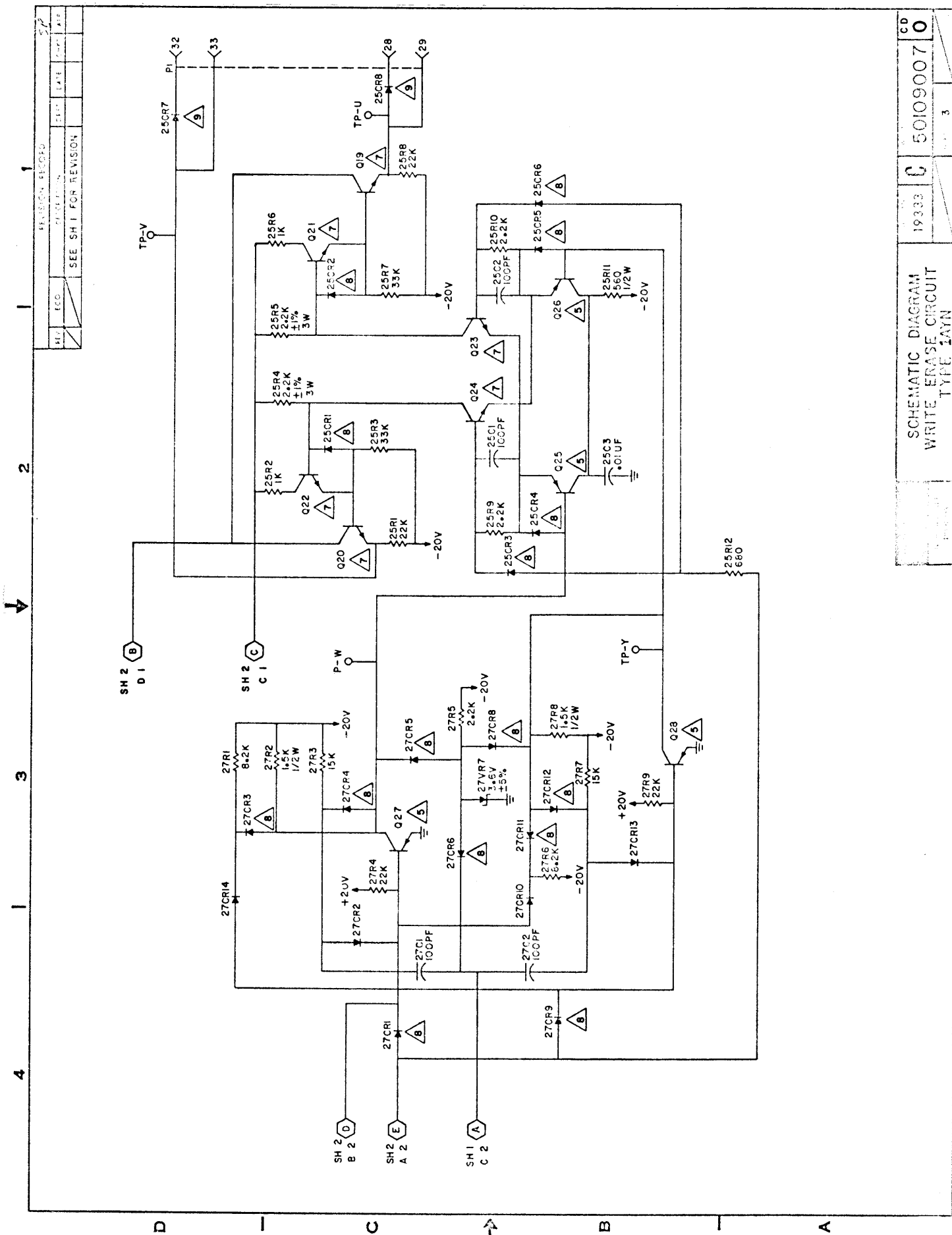
REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION	
COMP ASSY: 54098100		BR 2A1			
		CHK		4/12/71	
		ENGR		4/12/71	
		MFG		4/22/71	
		APPR		4/22/71	
COMPONENTS, EXCEPT AS NOTED		TOLERANCE		VALUE	
RES		±5%		OHMS 1/4 W	
CAP		±10%			
TITLE		SCHEMATIC DIAGRAM		DRAWING NUMBER	
TRACK SERVO FINE POSITION		TYPE ØAWW		CD	
CODE IDENT		19333		54098200	
SHEET 1 OF 3					

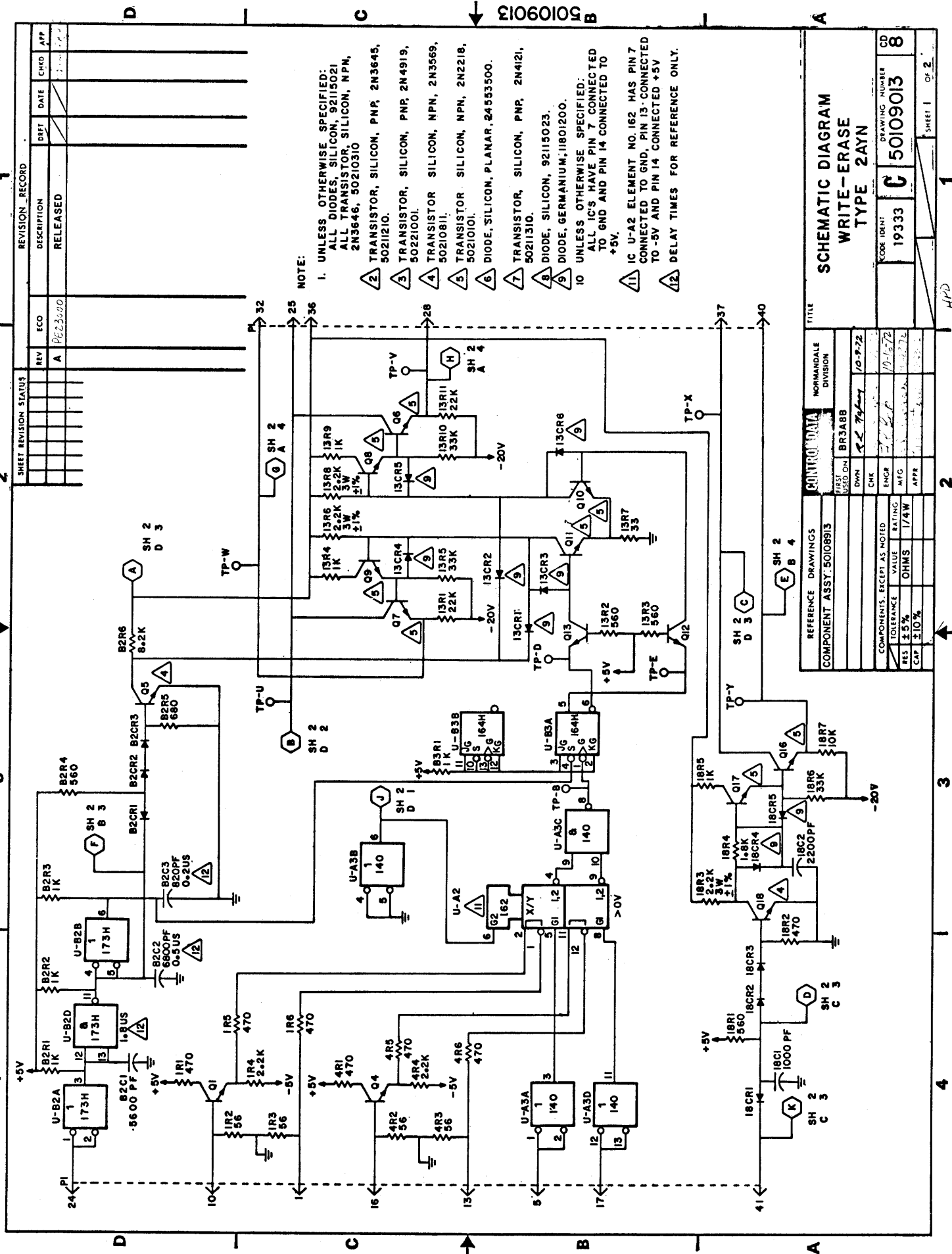




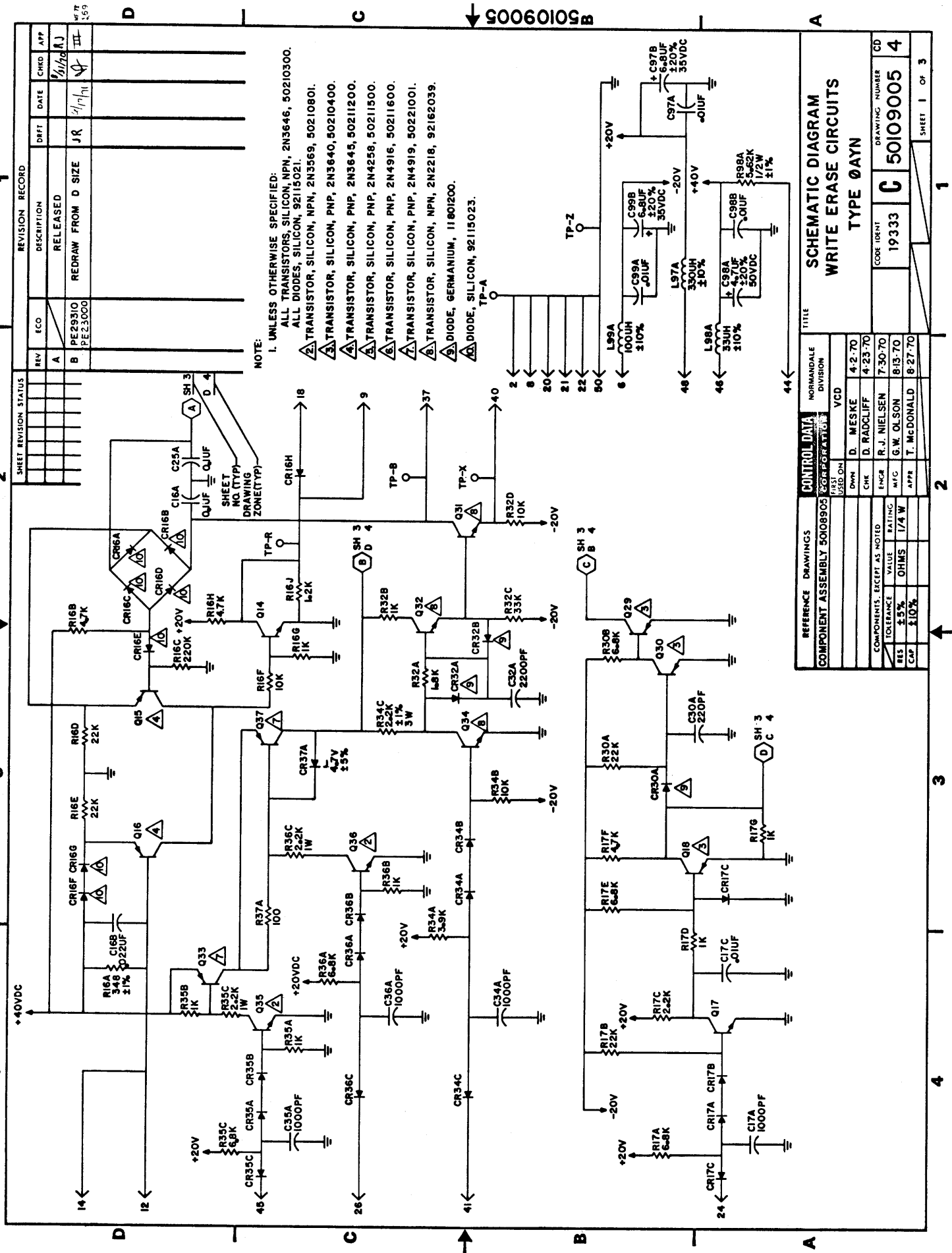


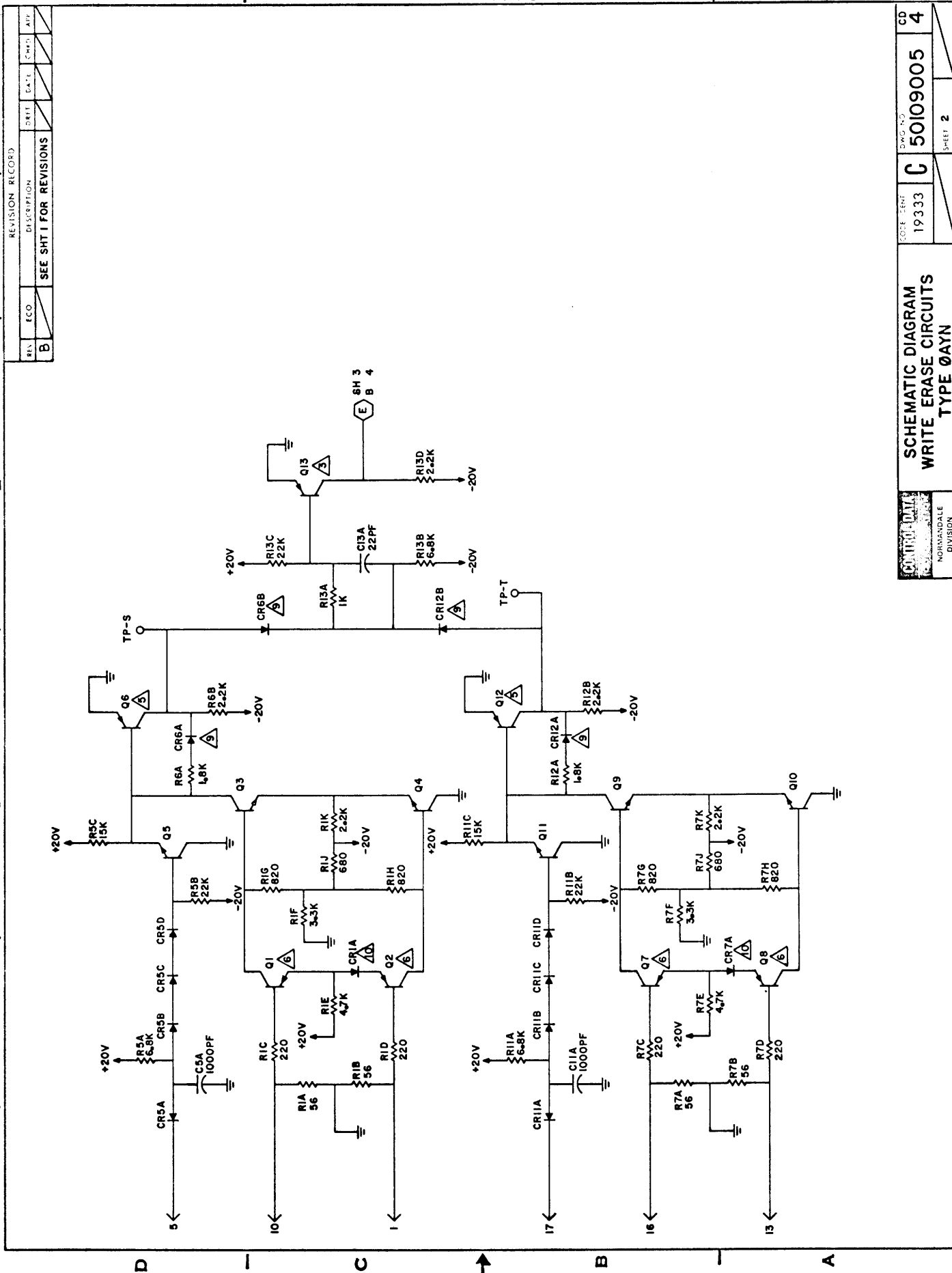




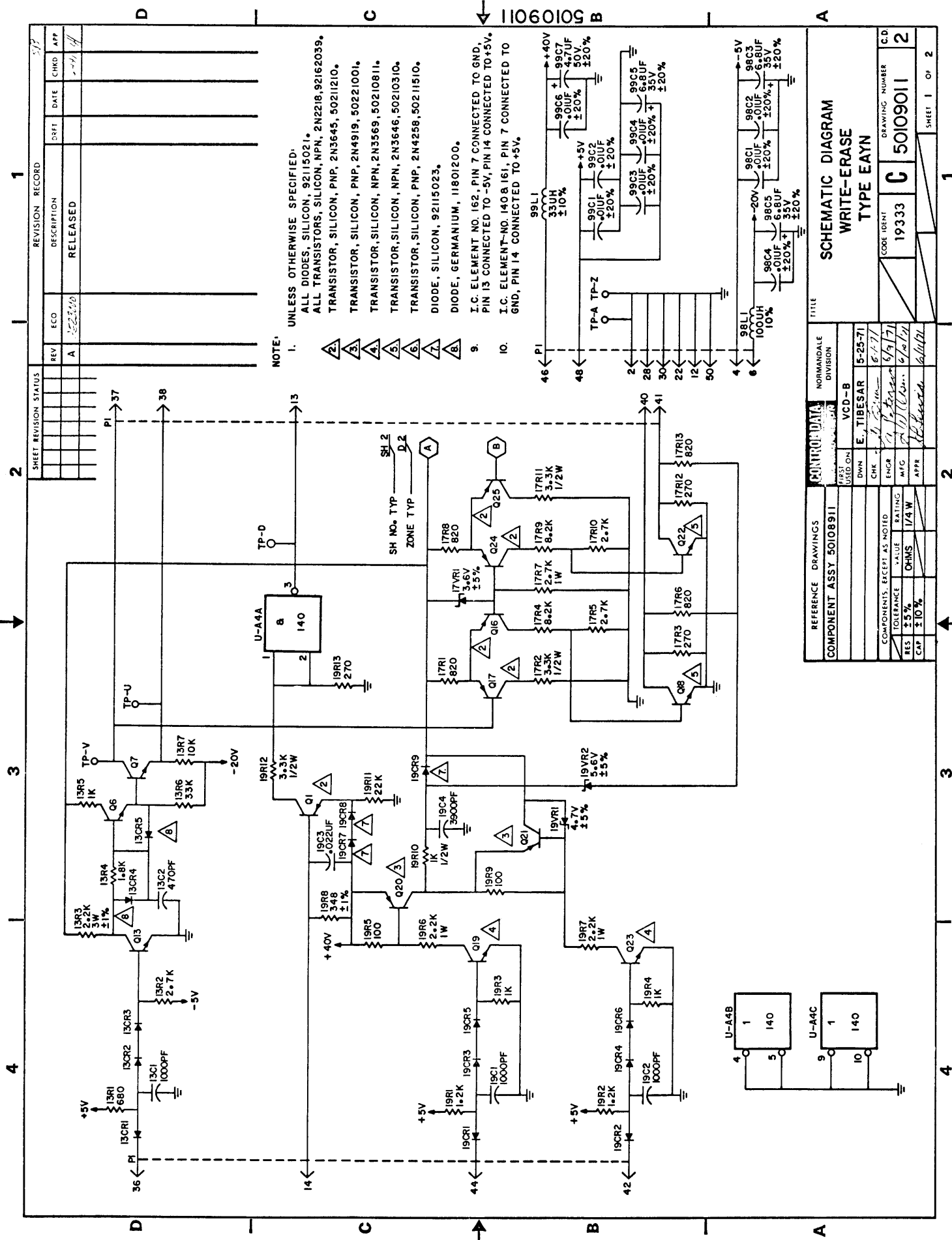


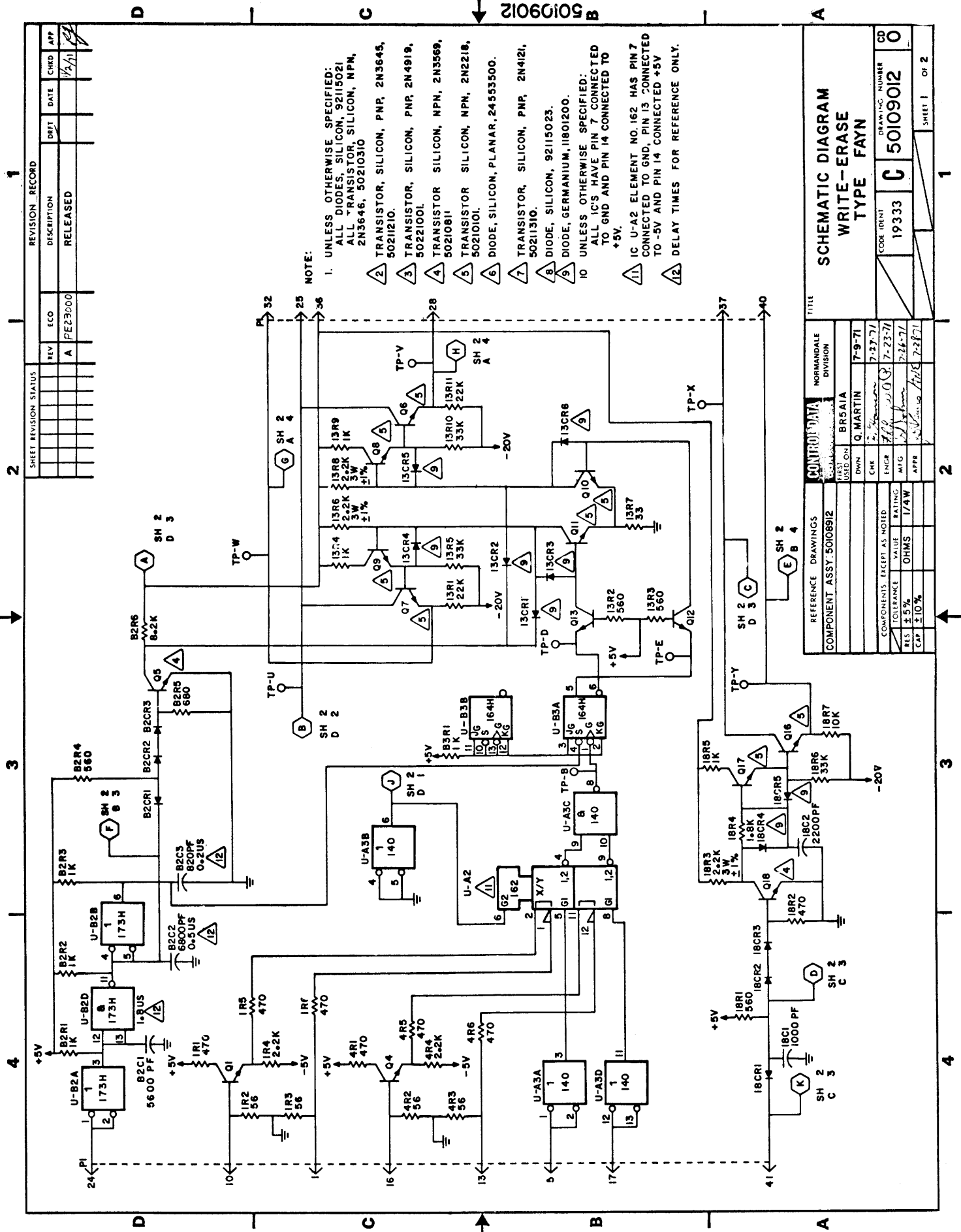


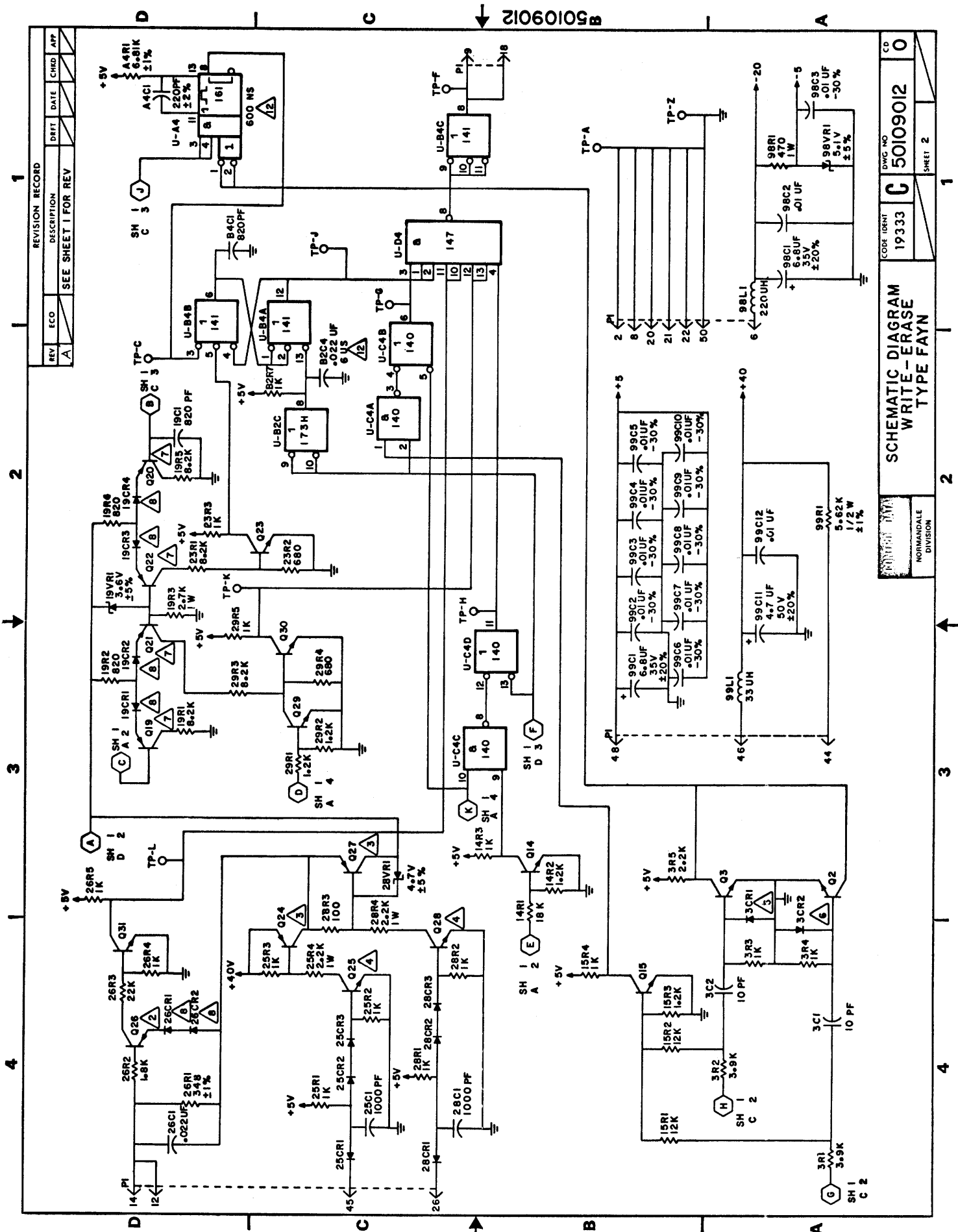


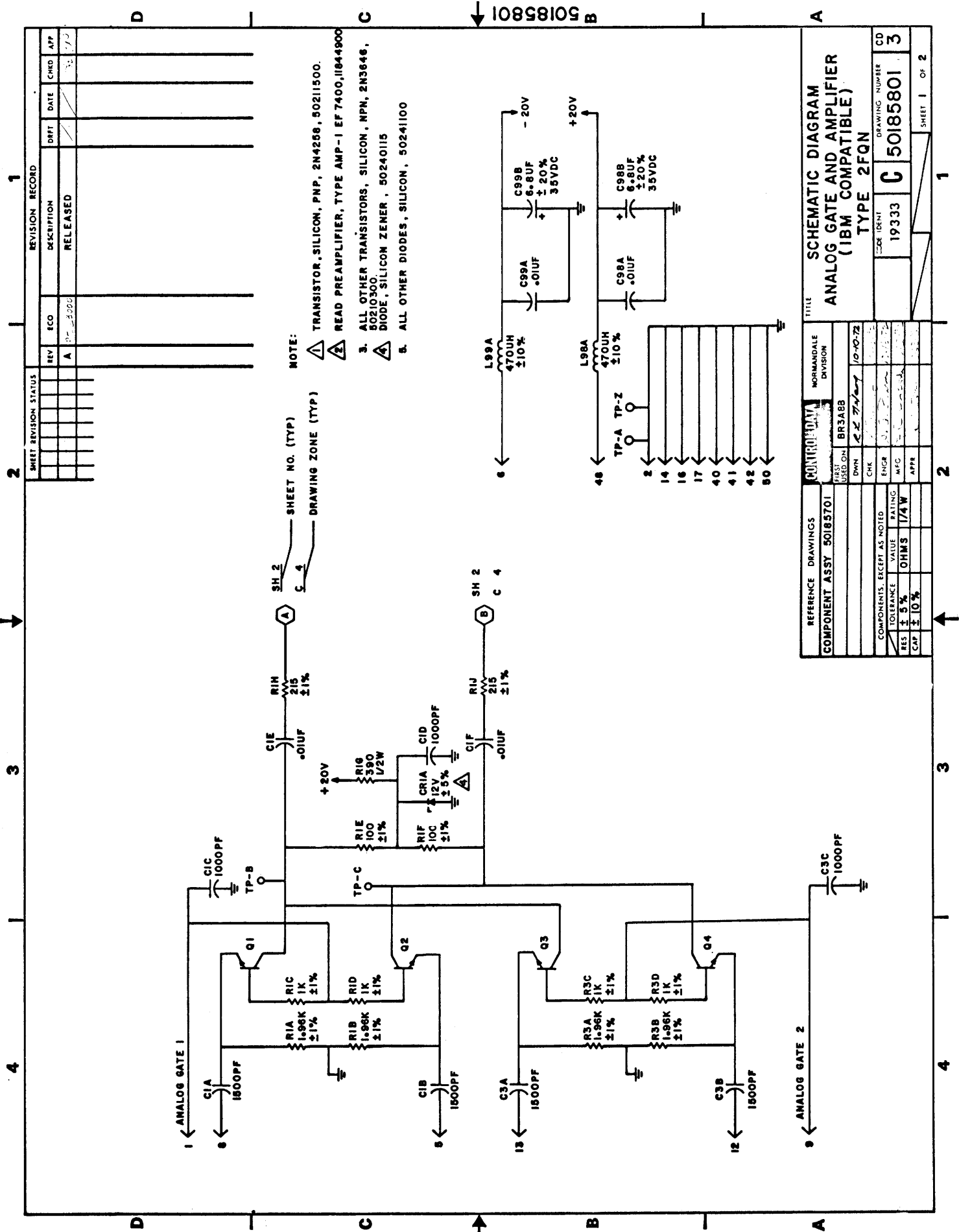


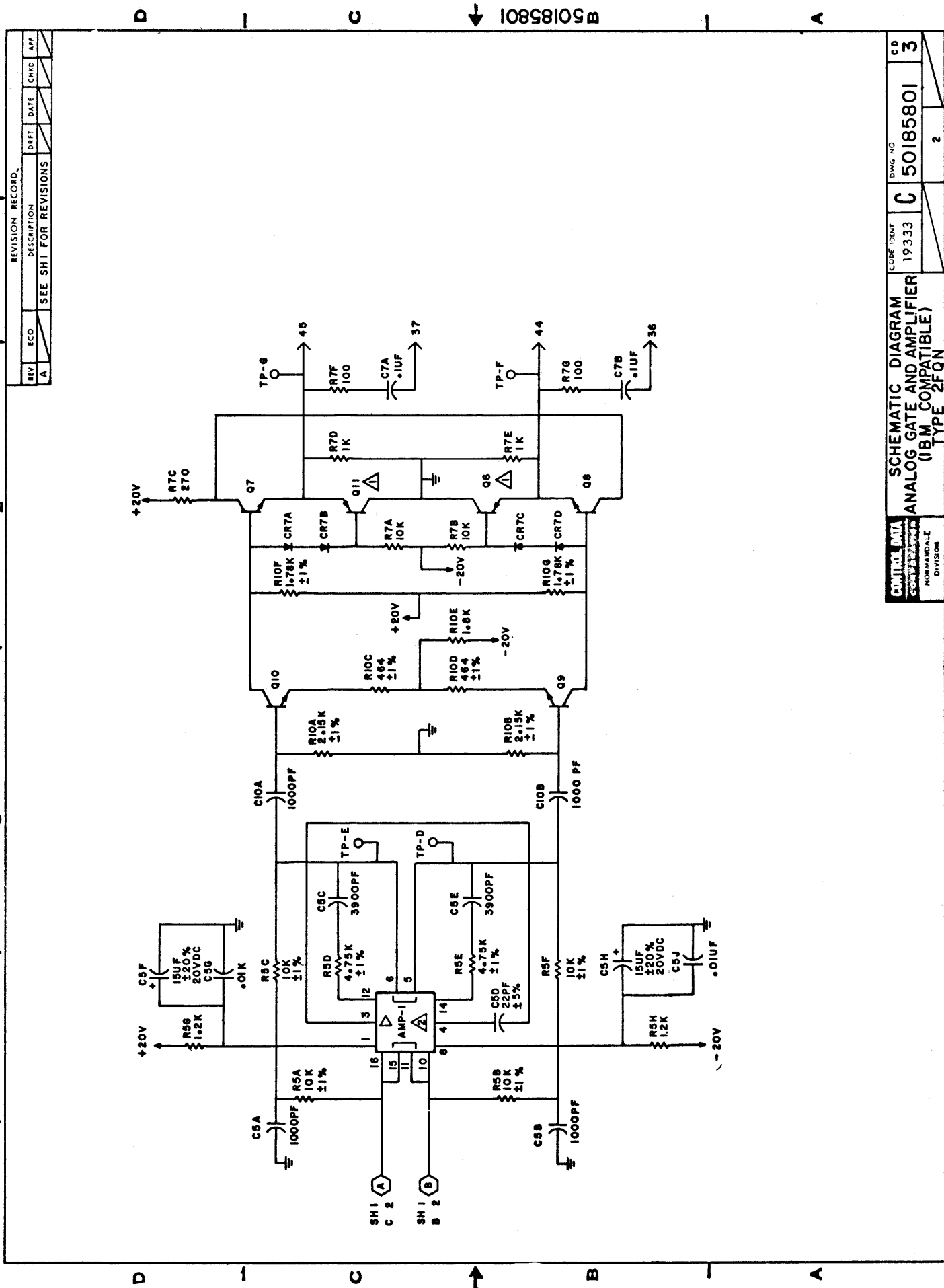
50109005





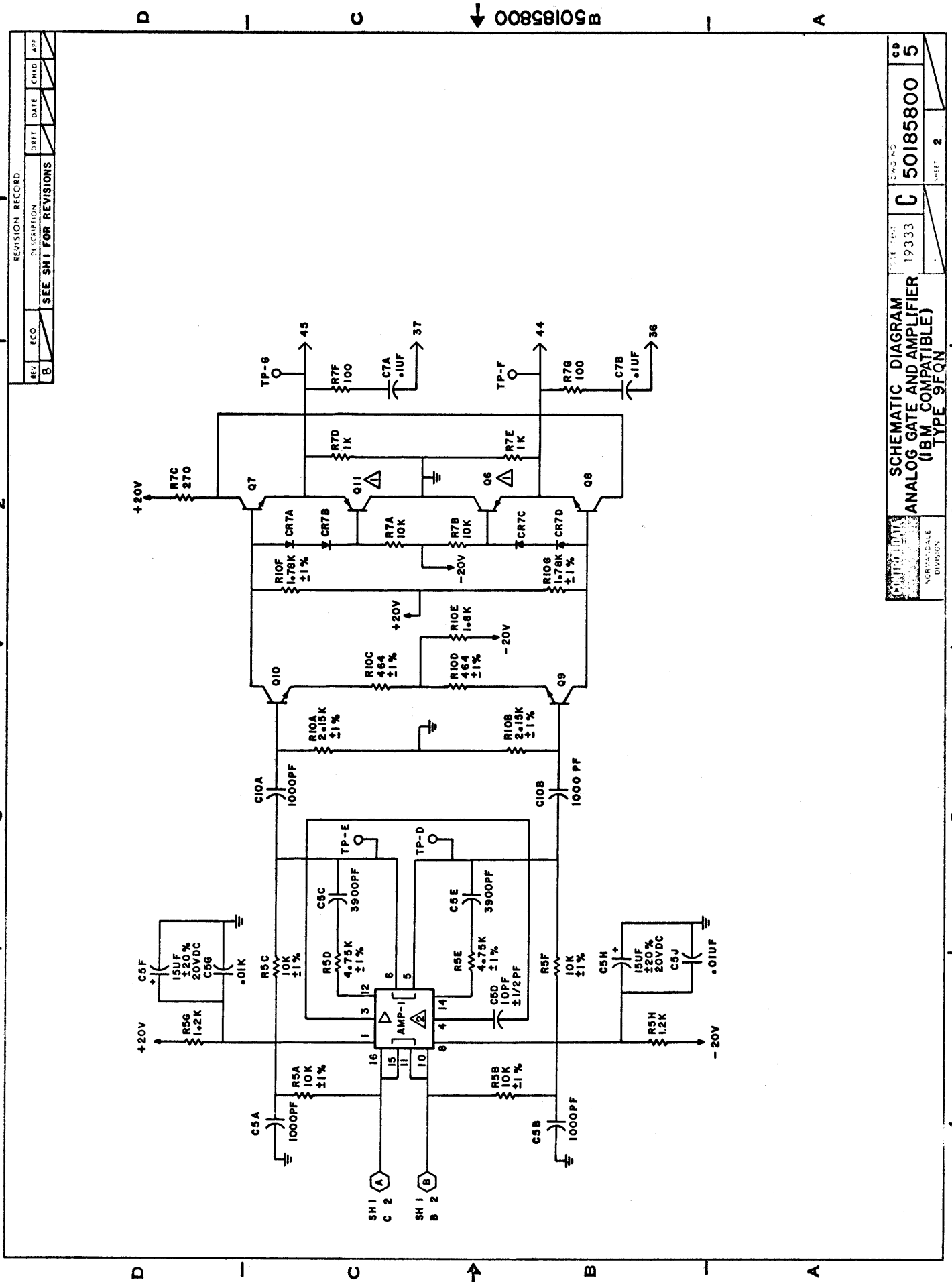


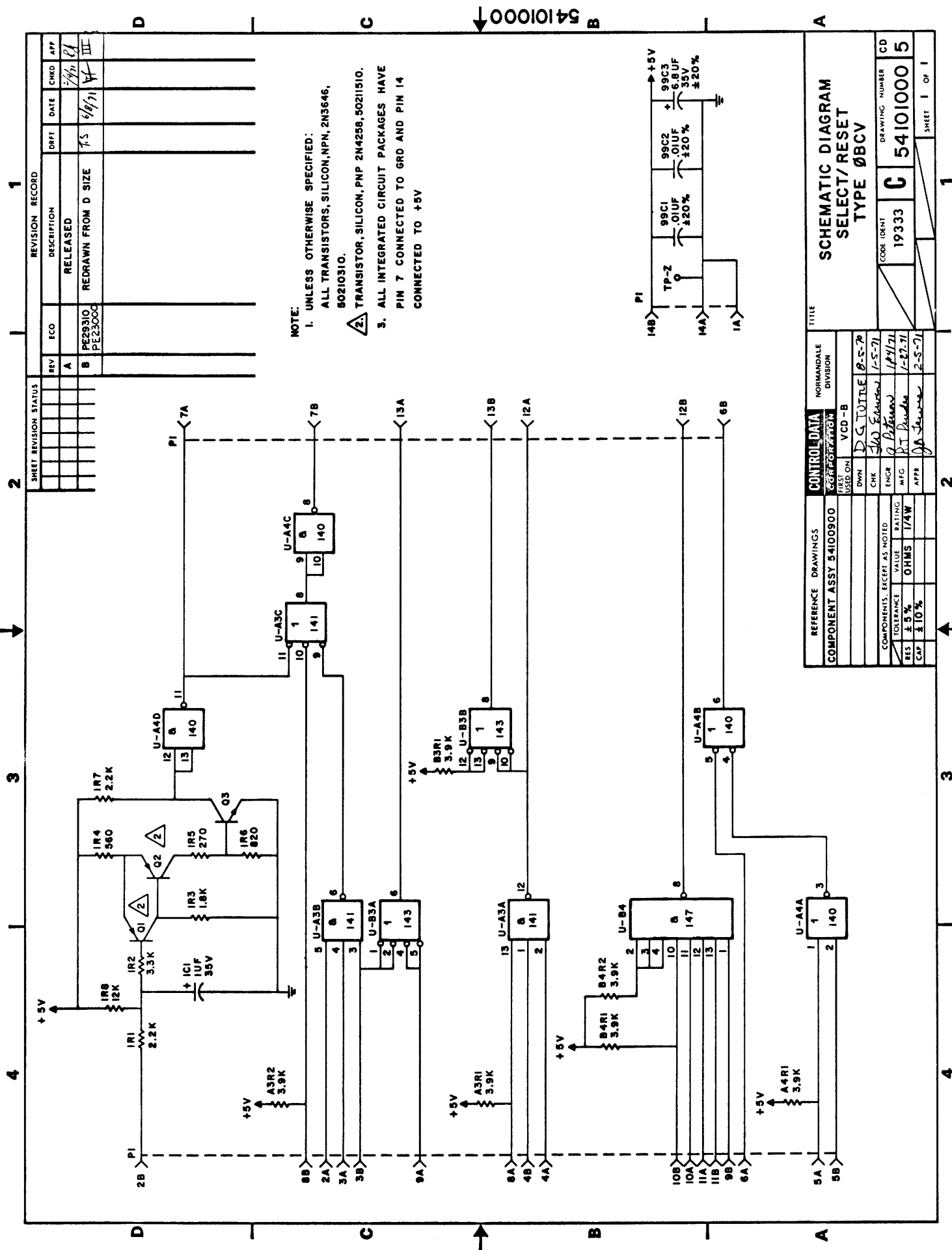


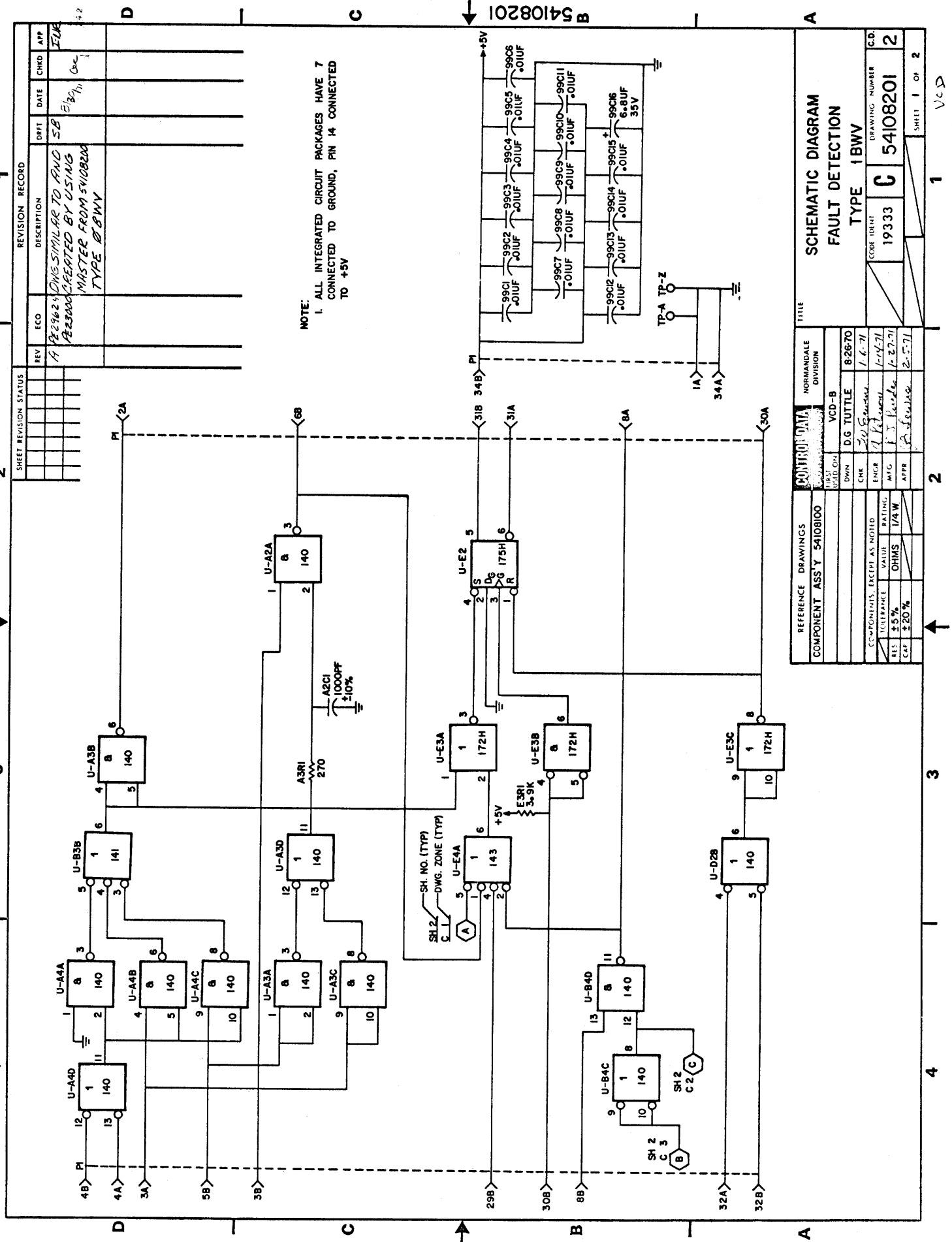


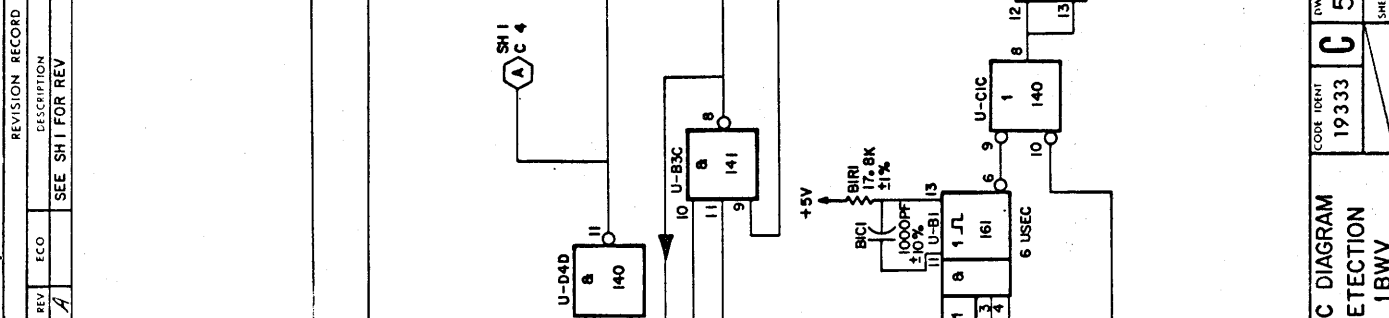


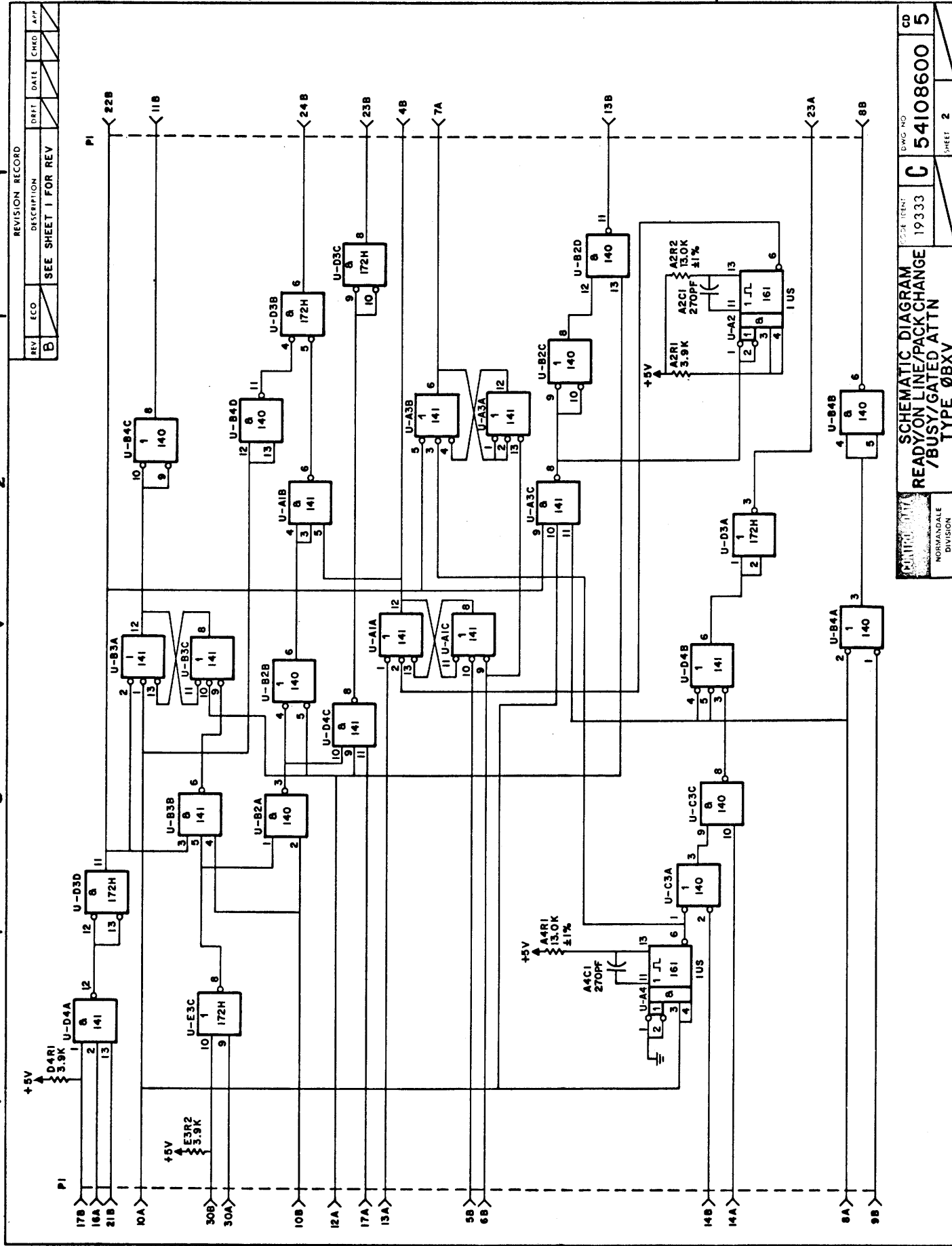
REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMPONENT ASSY 50185700		FIRST USED ON		DUAL CHANNEL		SCHEMATIC DIAGRAM	
		DWN		F. MANNING		ANALOG GATE AND AMPLIFIER (IBM COMPATIBLE)	
		CHK		P. J. COATS		TYPE 9FQN	
		ENGR		2-11-69		CODE IDENT	
		MFG		P. B. KENNEDY		19333	
		APPR		H. E. ARMBURG		DRAWING NUMBER	
						C 50185800	
COMPONENTS, EXCEPT AS NOTED		TOLERANCE		VALUE		5	
RES	± 5 %	OHMS		1/4 W			
CAP	± 10 %						
						SHEET 1 OF 2	

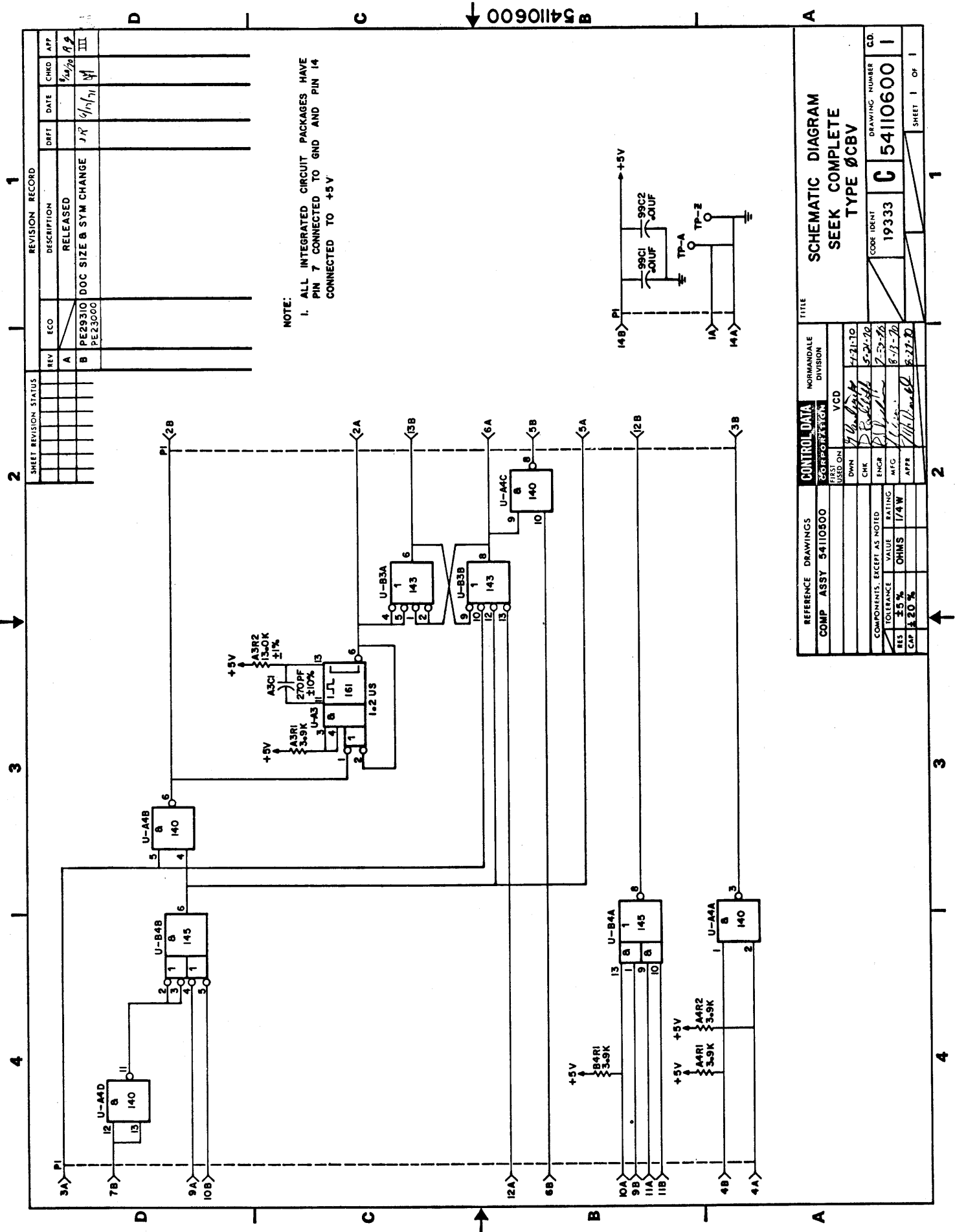


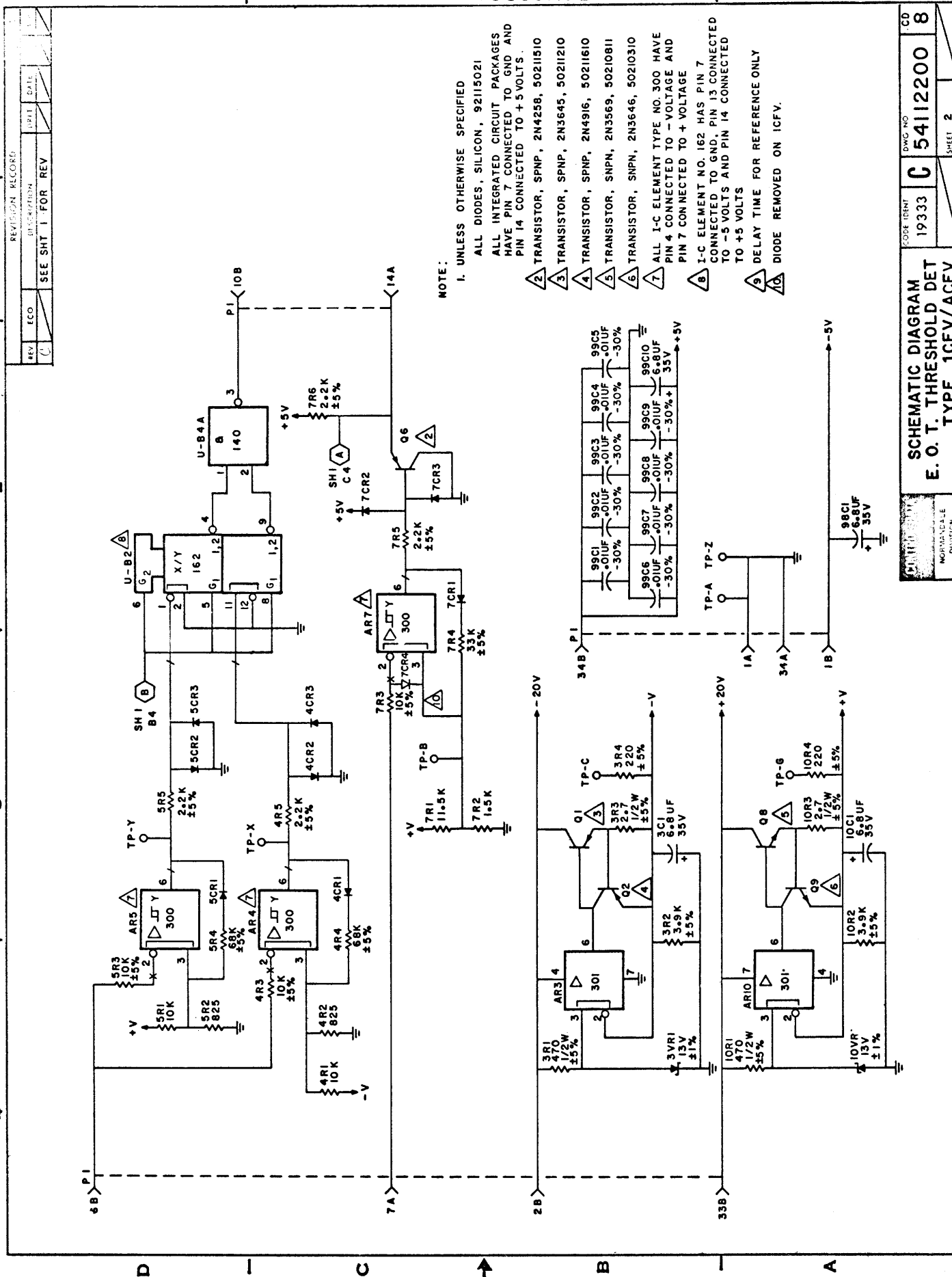


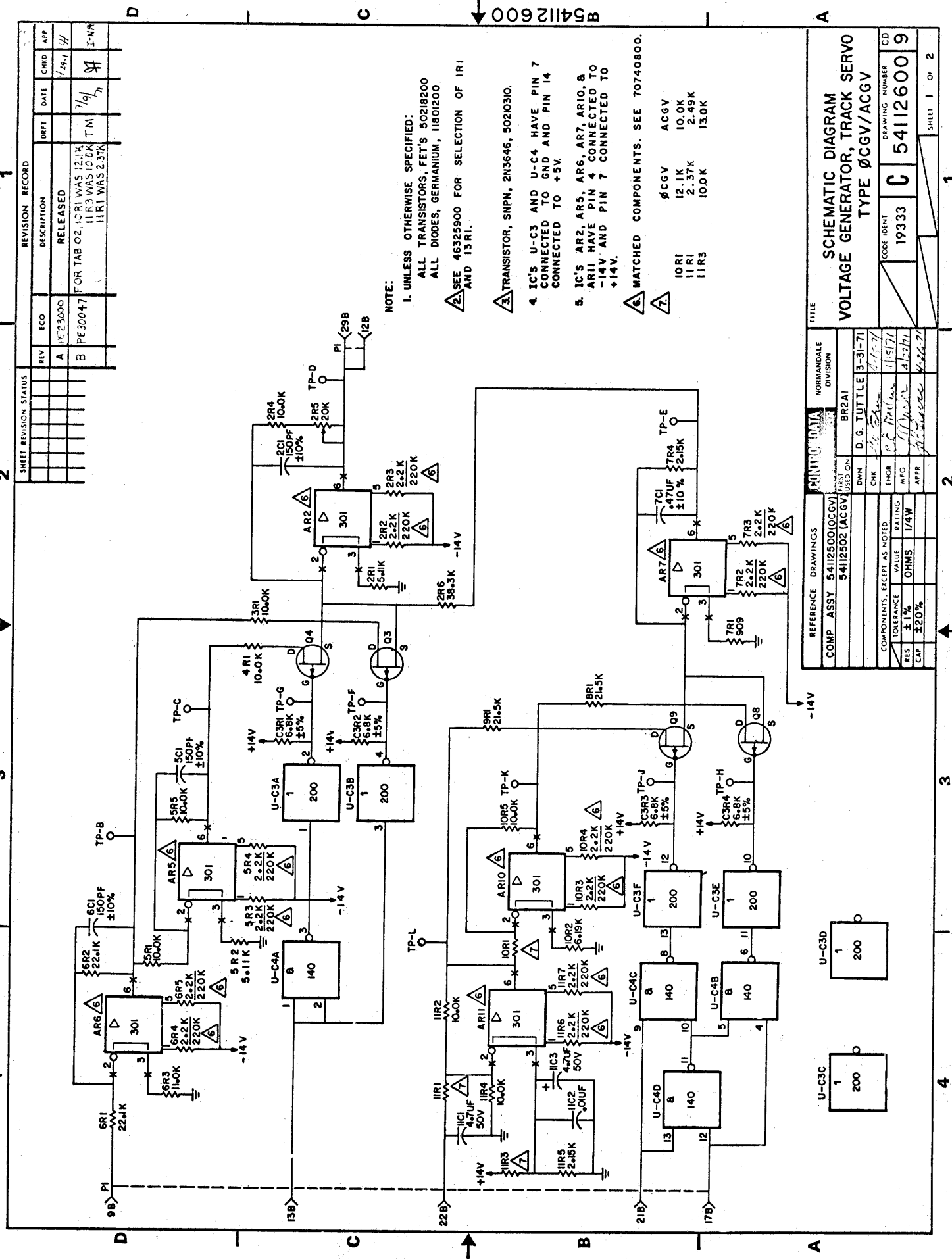












B54112600

A

TITLE

NORMANDALE

DIVISION

BR2A1

D. G. TUTTLE 3-31-71

CHK

DWN

ENGR

MFG

APPR

COMPONENTS, EXCEPT AS NOTED

TOLERANCE

VALUE

RATING

OHMS

1/4W

CAP

±20%

RES

±1%

CORE IDENT

19333

DRAWING NUMBER

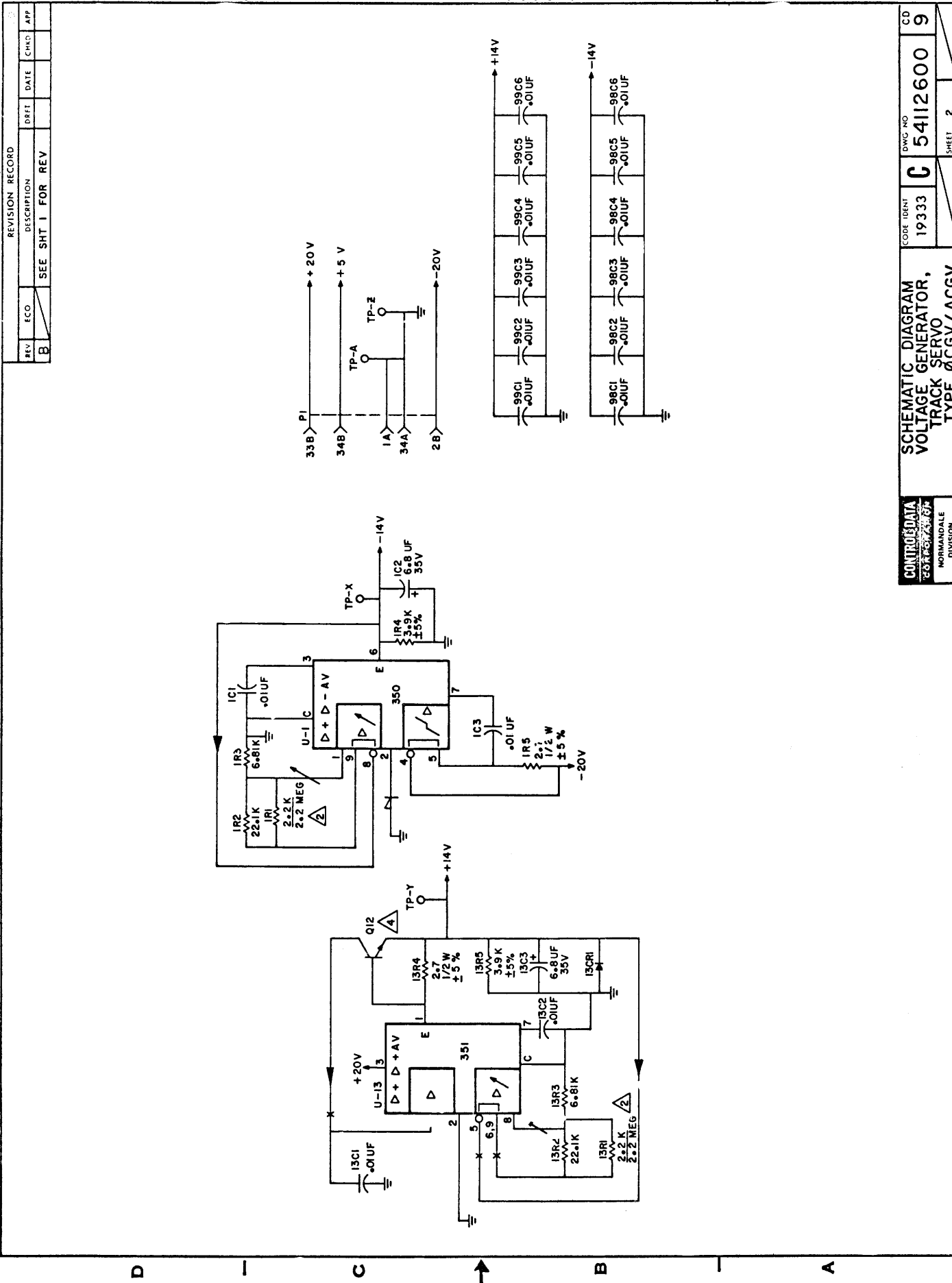
54112600

CD

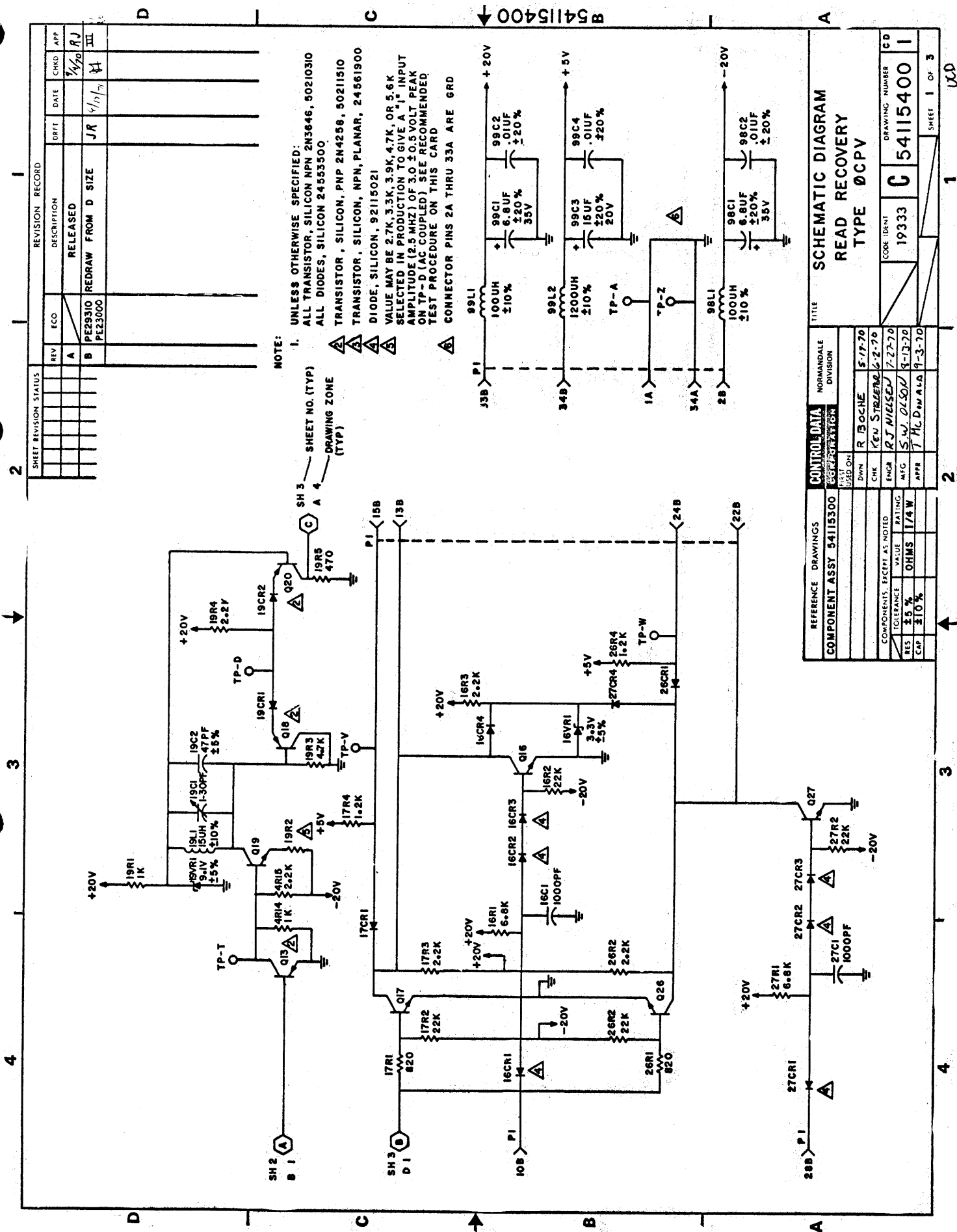
9

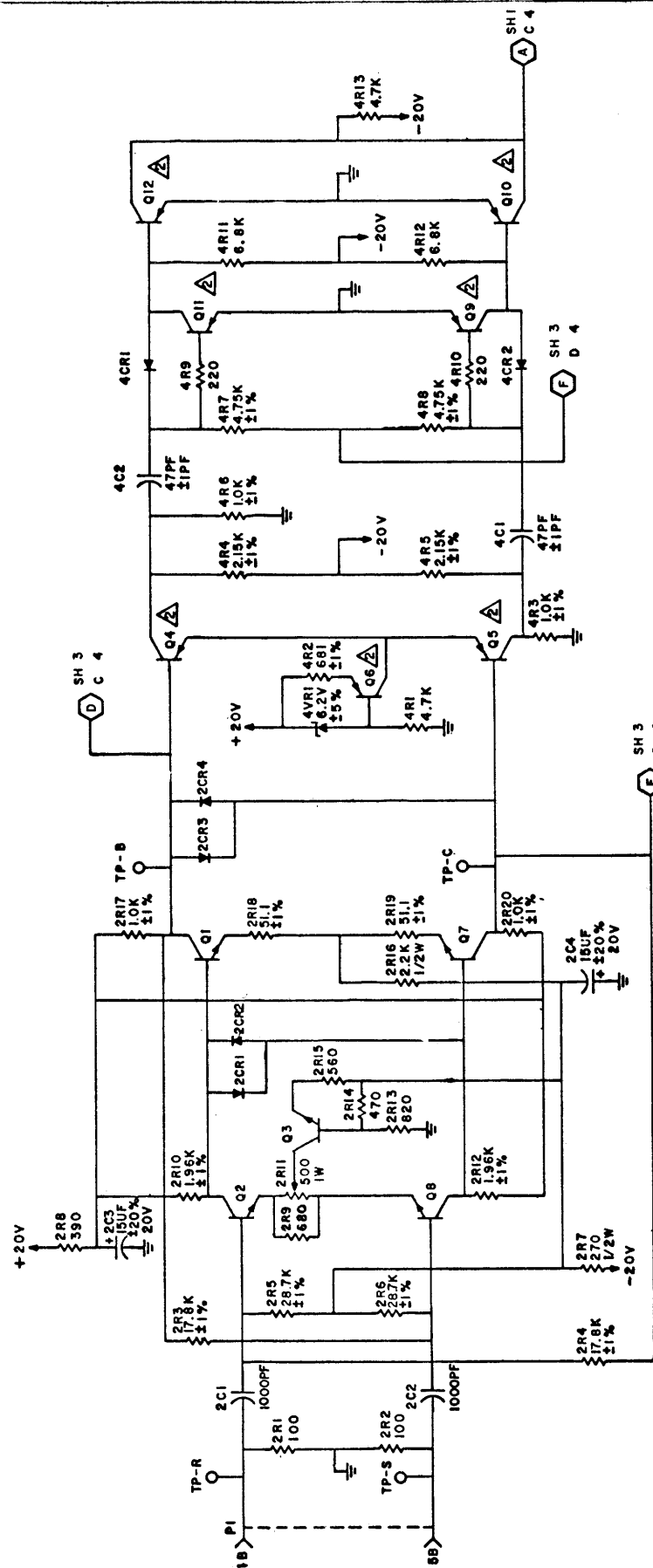
SHEET 1 OF 2

1



54112600





SCHEMATIC DIAGRAM
READ RECOVERY
TYPE ØCPV

19323	C	54115400
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10

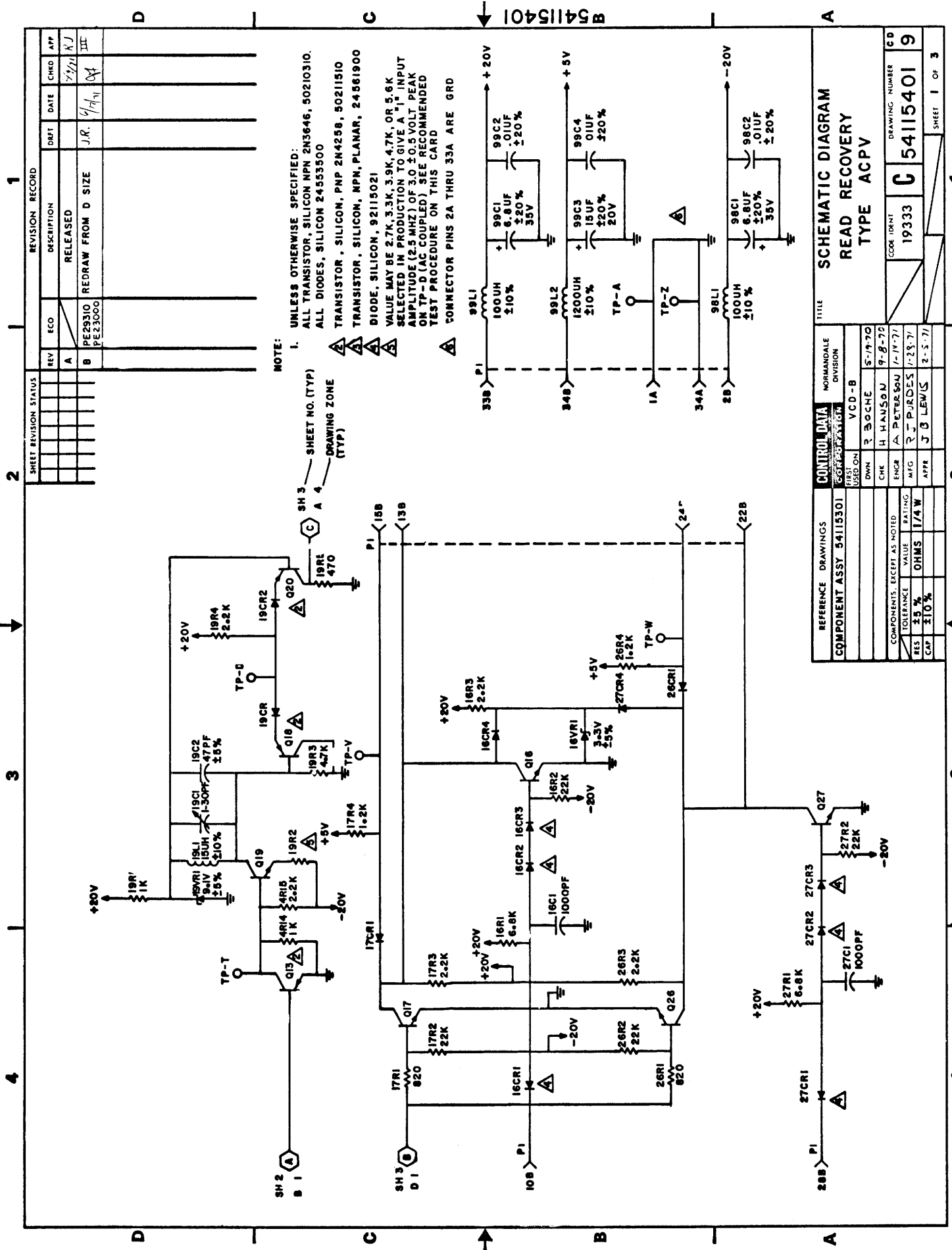
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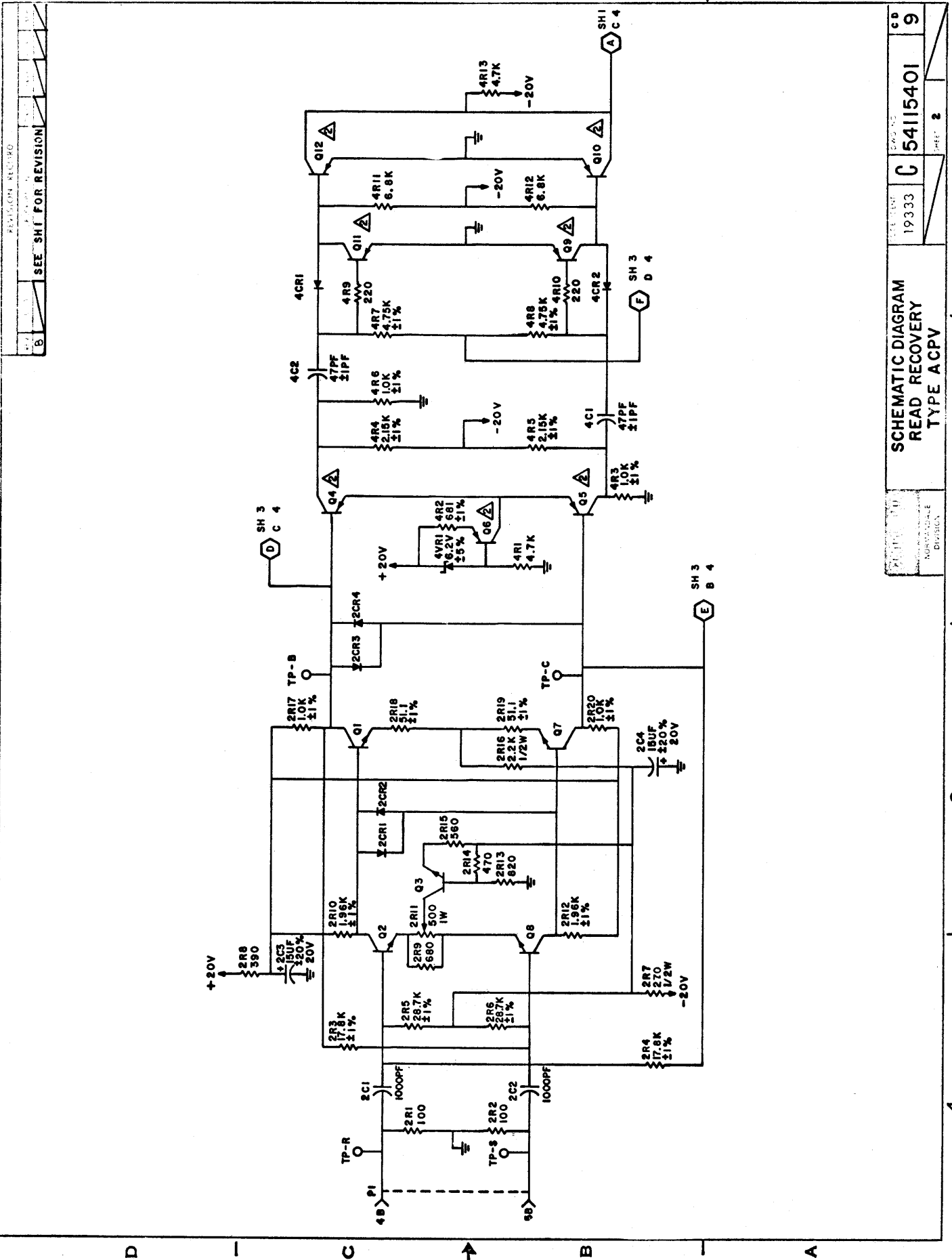
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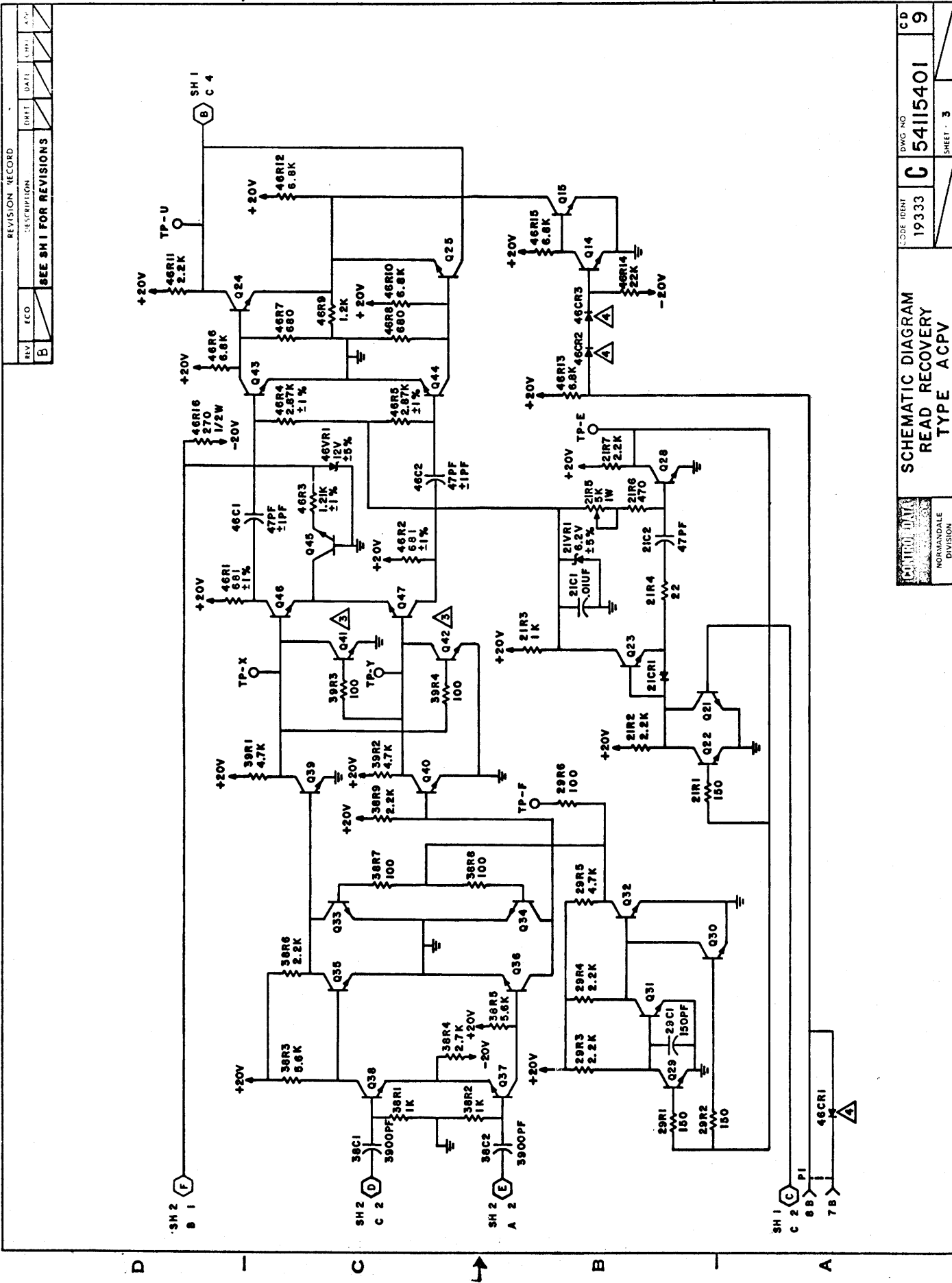
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6

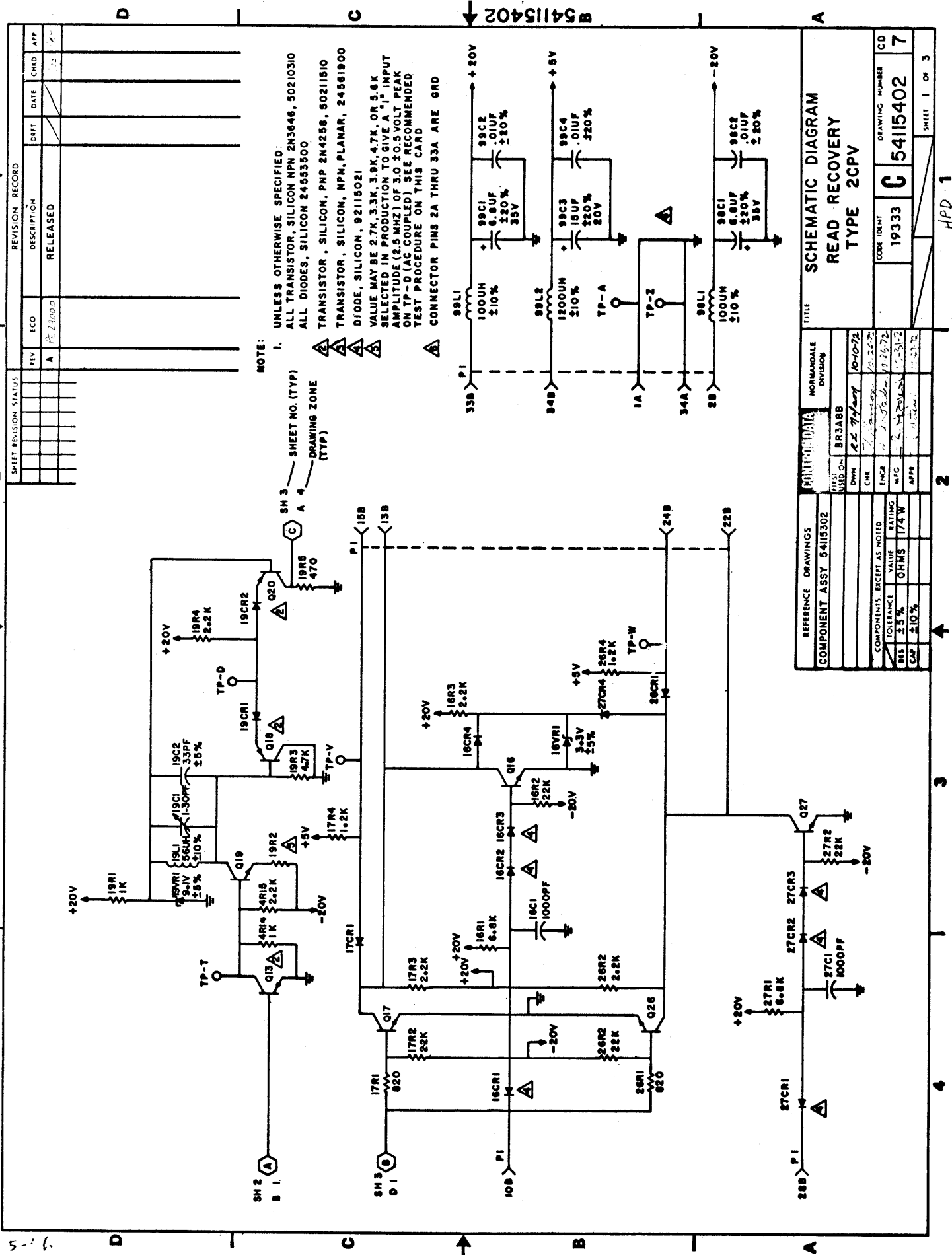
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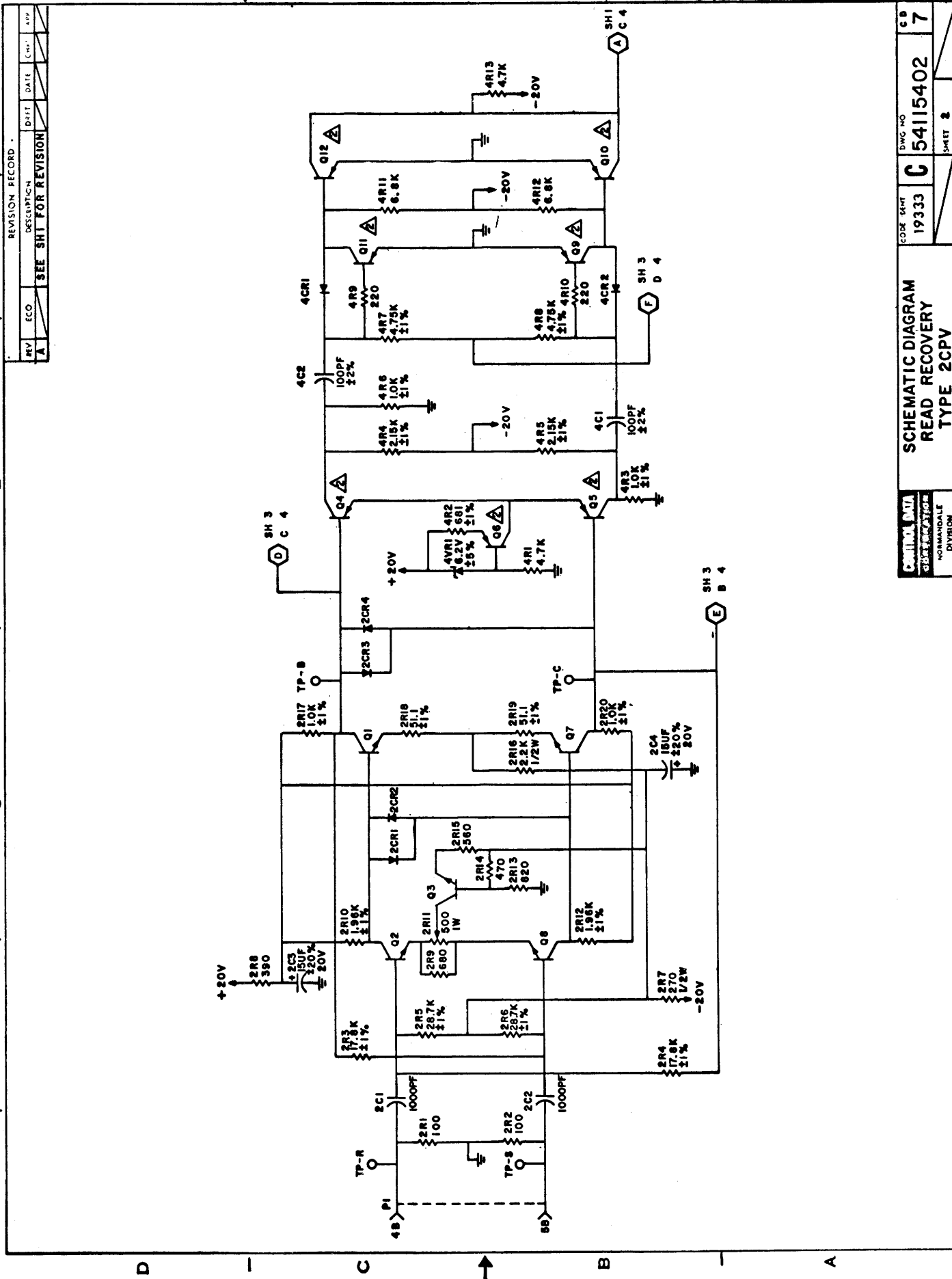






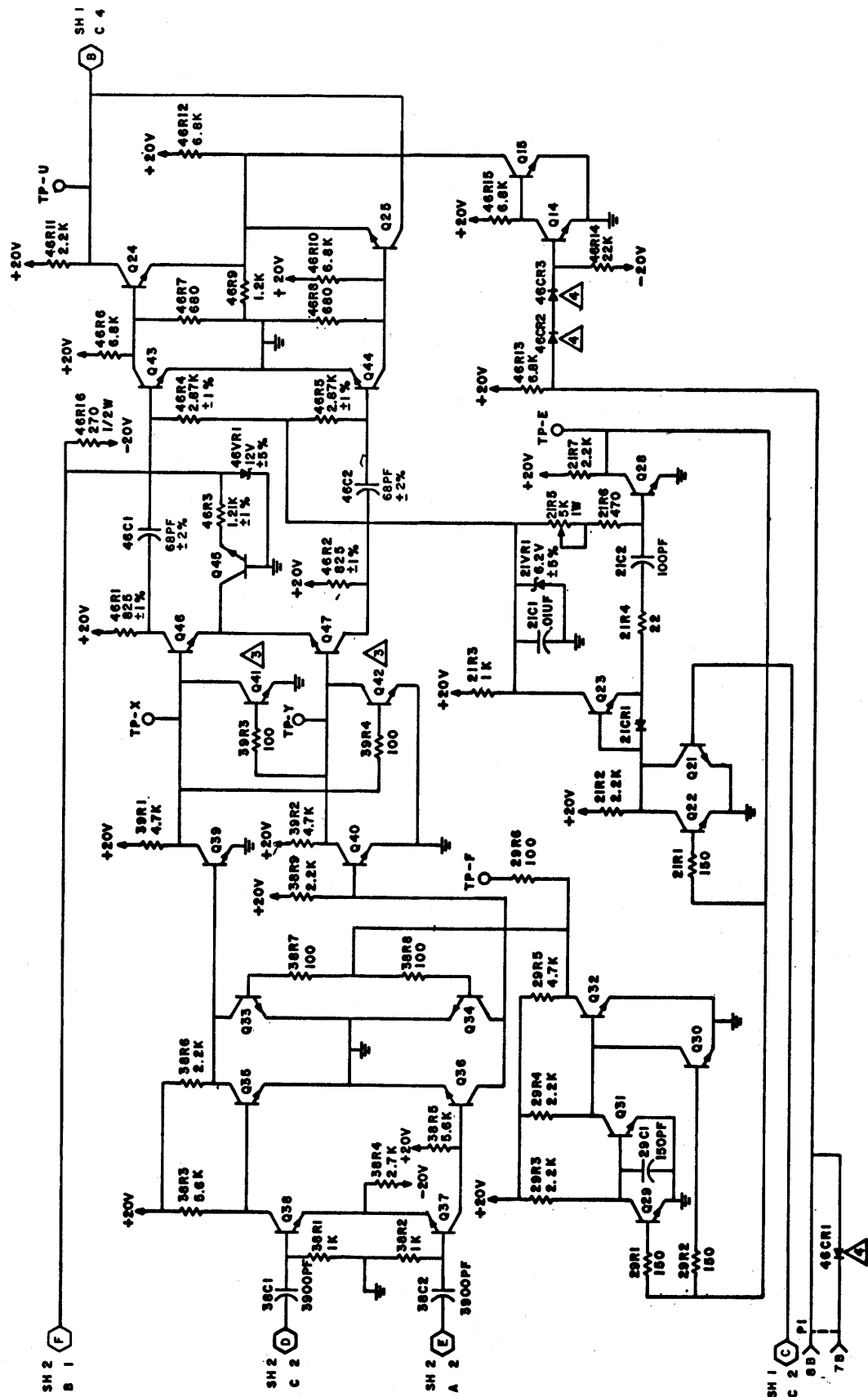
1 2 3 4





B 54115402

REVISION RECORD			
REV	ECO	DESCRIPTION	DATE
A		SEE SH 1 FOR REVISIONS	



SCHEMATIC DIAGRAM
READ RECOVERY
TYPE 2CPV

CONTROL DATA
CORPORATION
HUNTSVILLE
DIVISION

CODE 104RT
19333

54115402

CD

SHEET 3

1

2

3

4

SHEET REVISION STATUS		REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD
A		RELEASED			
B		REDRAWN FROM D SIZE	1.5	4/8/71	

REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION	
COMPONENT ASS'Y 54115801		CORPORATION		DSU-A	
FIRST USED ON		DWN		K STEETER 10-15-70	
CHKR		CHKR		H HANSON 10-24-70	
COMPONENTS, EXCEPT AS NOTED		ENGR		R J. J. J. J. 10-24-70	
TOLERANCE		VALUE		RFG	
CAP		RATING		MFG	
RES		APPR		T. McDaniel 11/4/70	

TITLE		SCHEMATIC DIAGRAM	
JUMPER		TYPE 1CQV	
CODE IDENT		19333	
DRAWING NUMBER		54115801	
SHEET 1 OF 1			

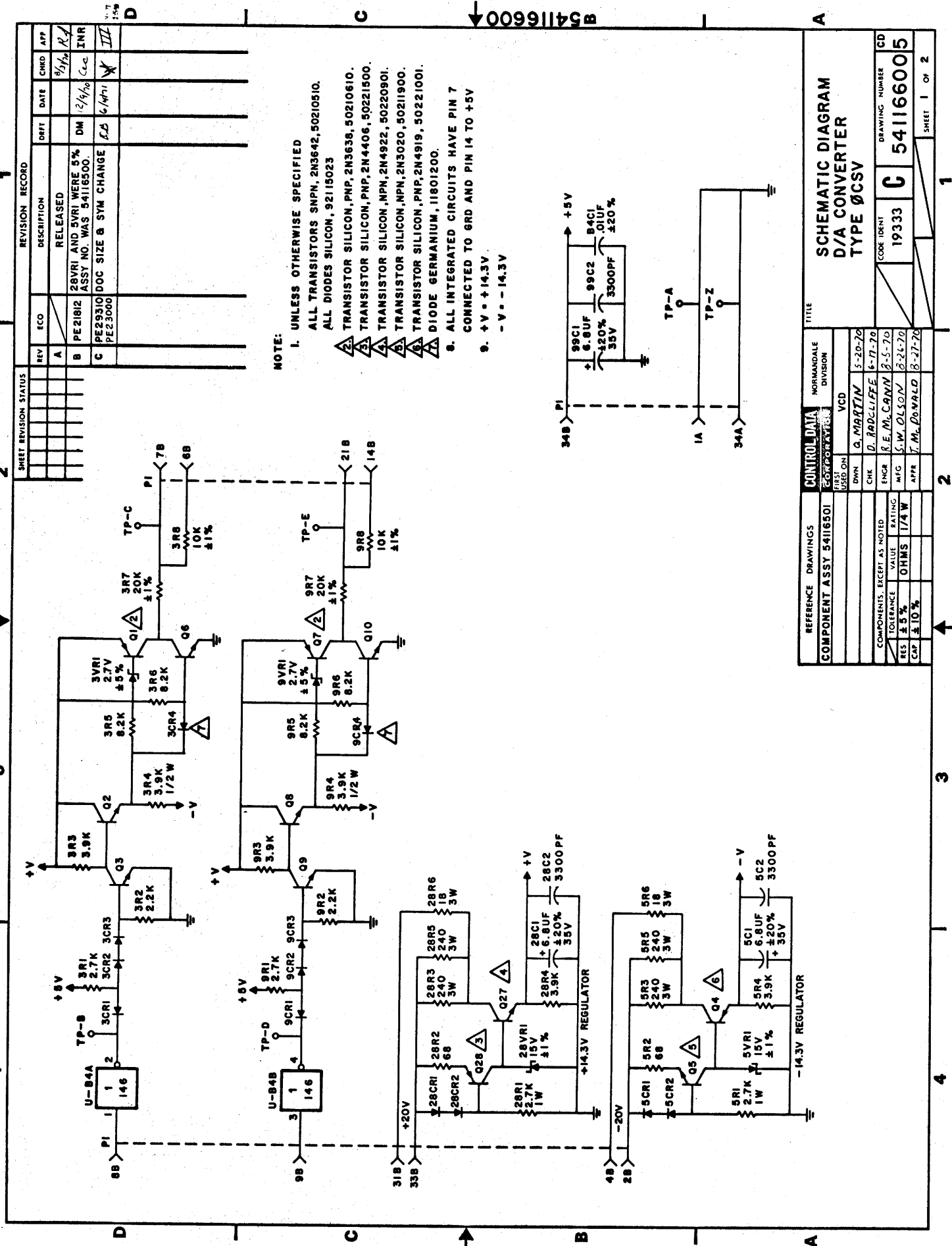
B 54115801

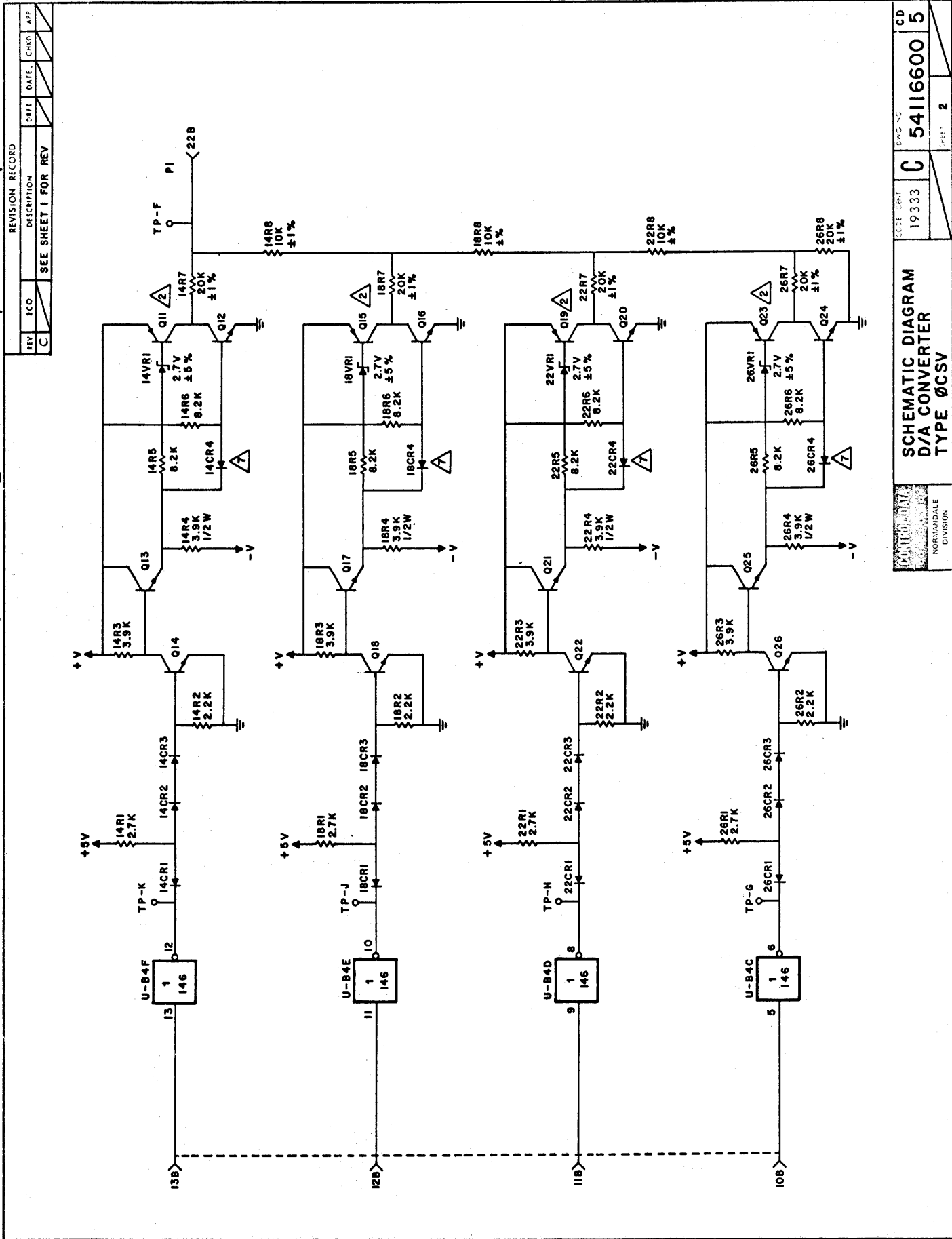
4

3

2

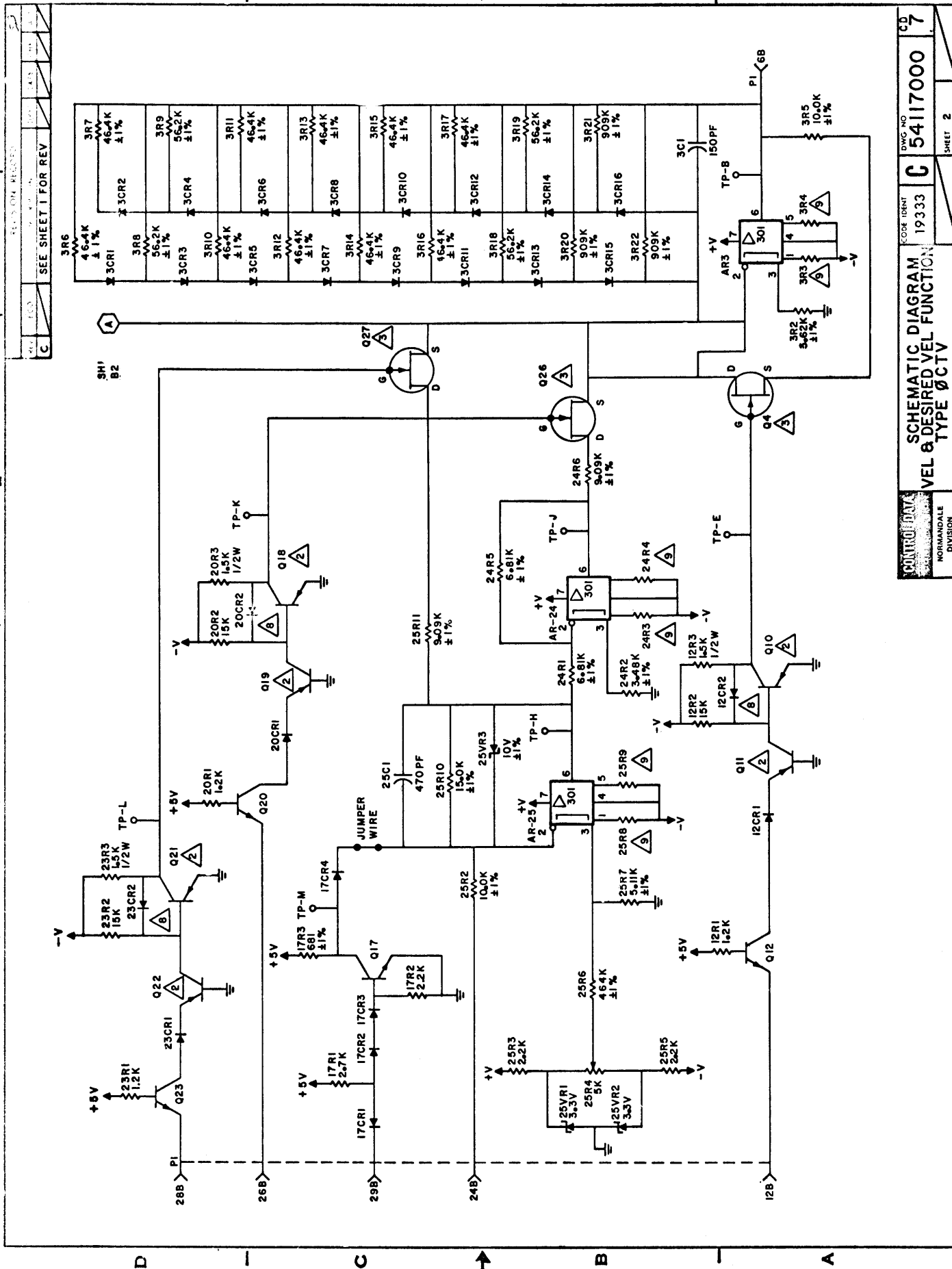
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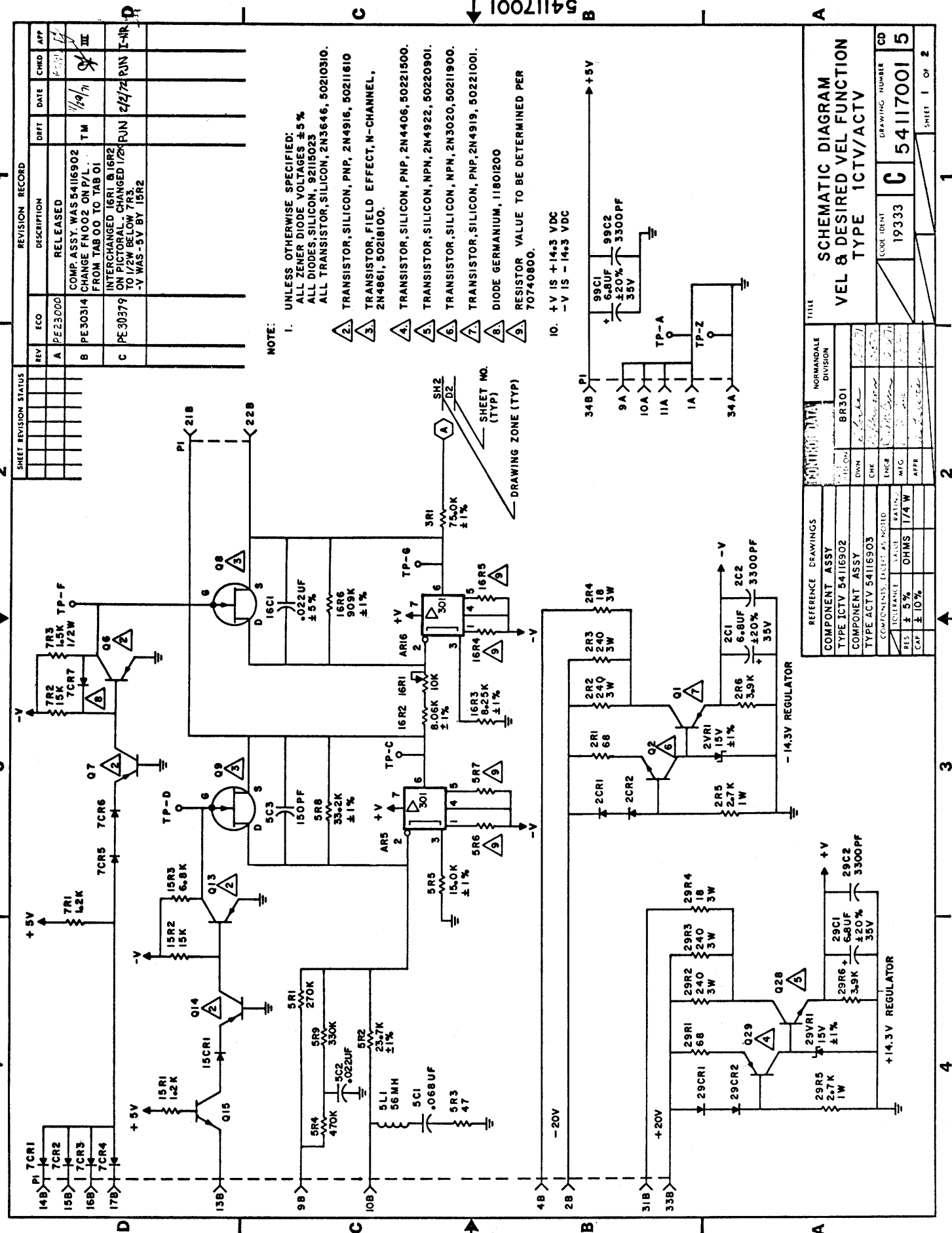




SCHEMATIC DIAGRAM		CD	
D/A CONVERTER		54116600 5	
TYPE 0CSV		1933	
NORMANDALE DIVISION		2	

REVISION RECORD			
REV	ECO	DESCRIPTION	DATE
1	C	SEE SHEET 1 FOR REV	

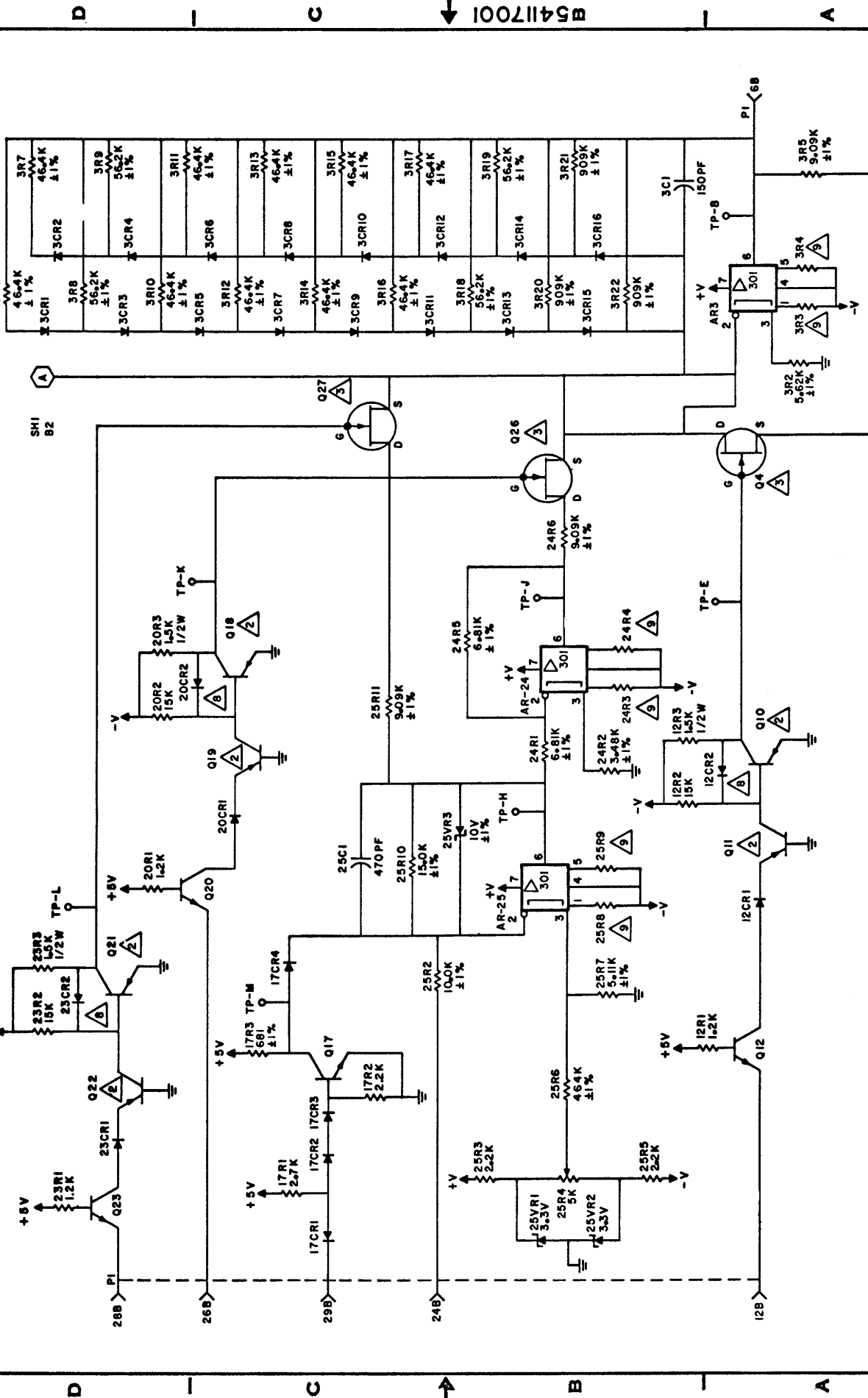




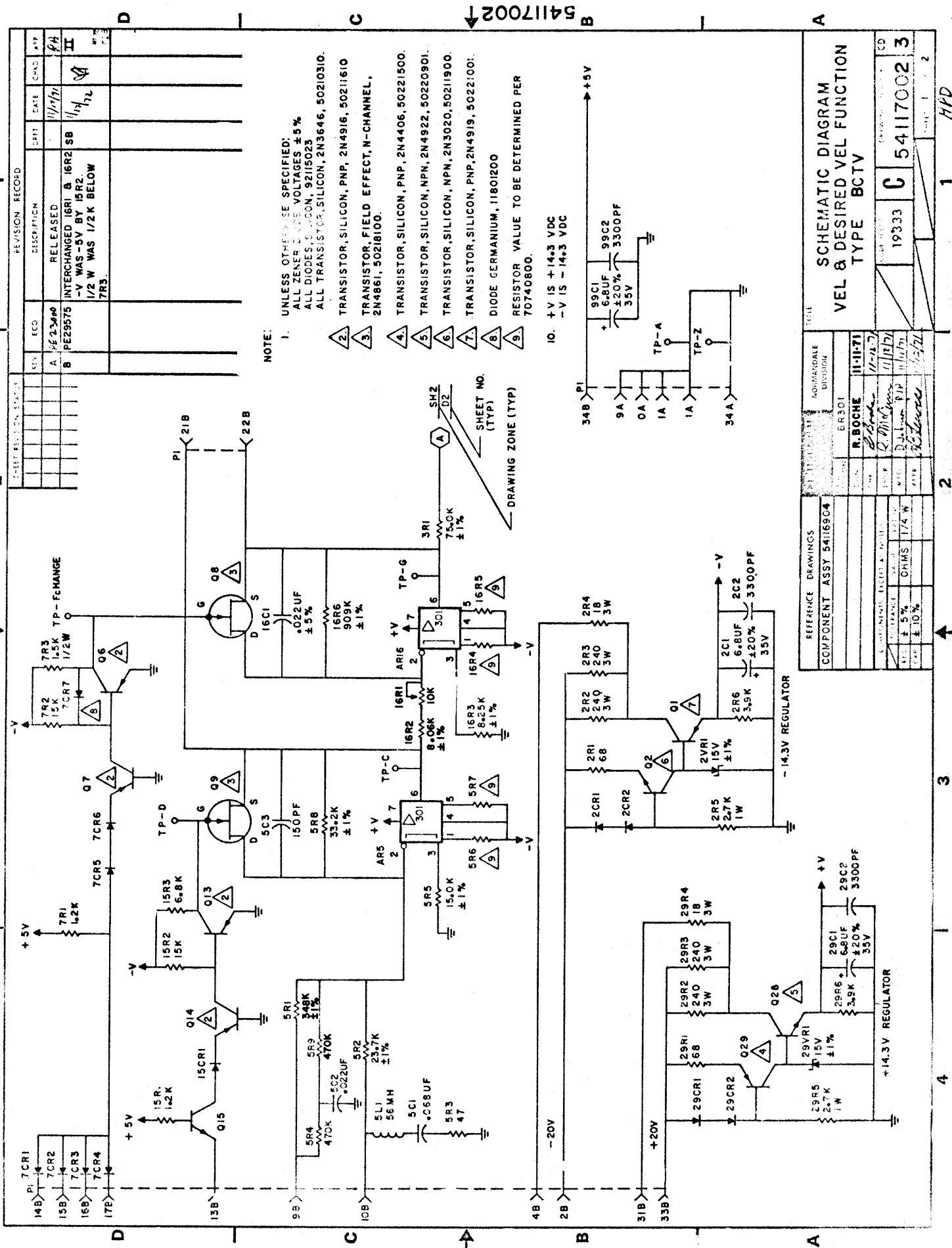
REVISION RECORD			
REV	ECO	DESCRIPTION	DATE
C		SEE SHEET 1 FOR REV	

REV	ECO	DESCRIPTION	DATE
C		SEE SHEET 1 FOR REV	

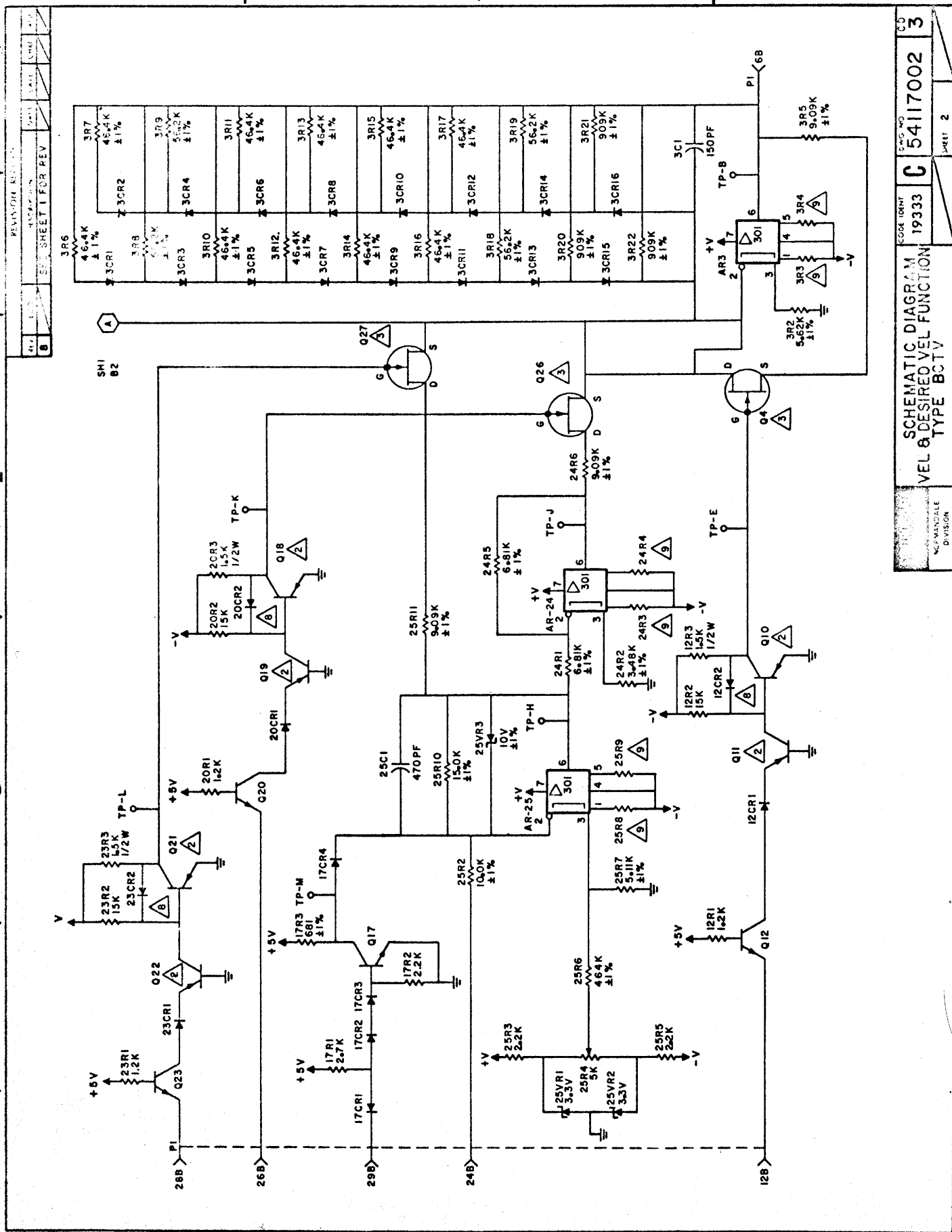
7-130.2



SCHEMATIC DIAGRAM	54117001	5
VEL & DESIRED VEL FUNCTION	19333	
TYPE 1CTV/ACTV		
NORM SCALE		
DIVISION		
SHEET 2		

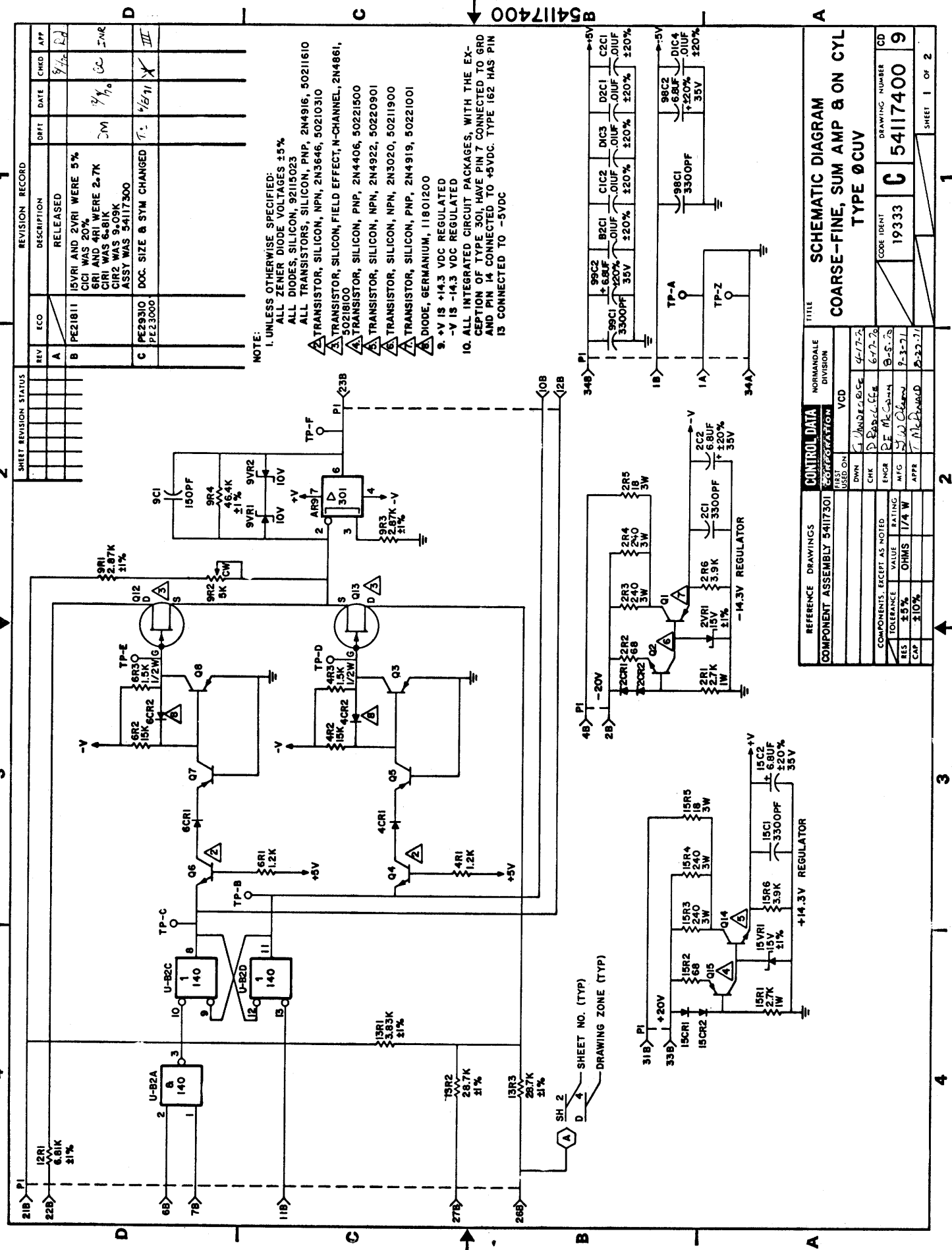


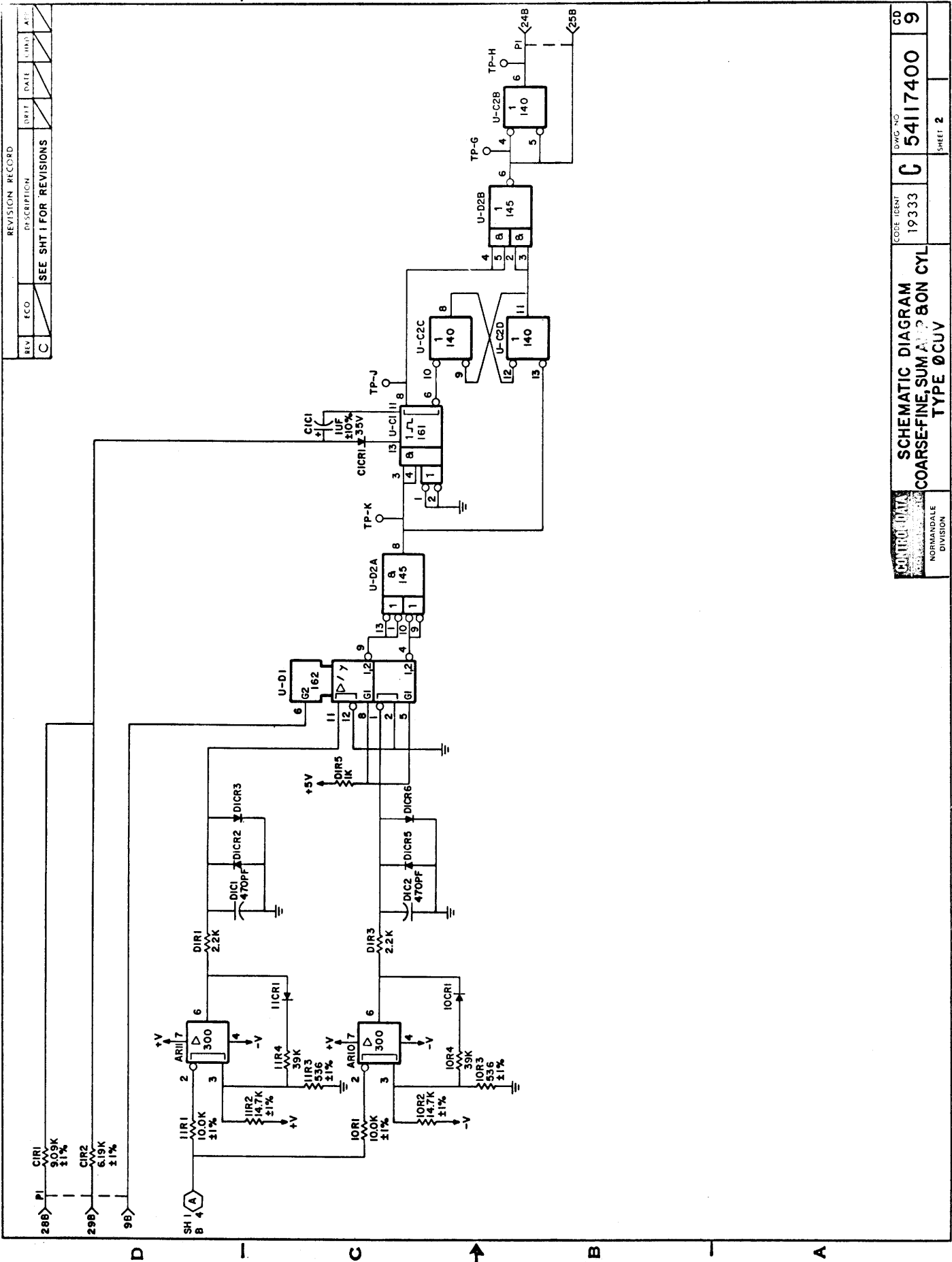
54117002

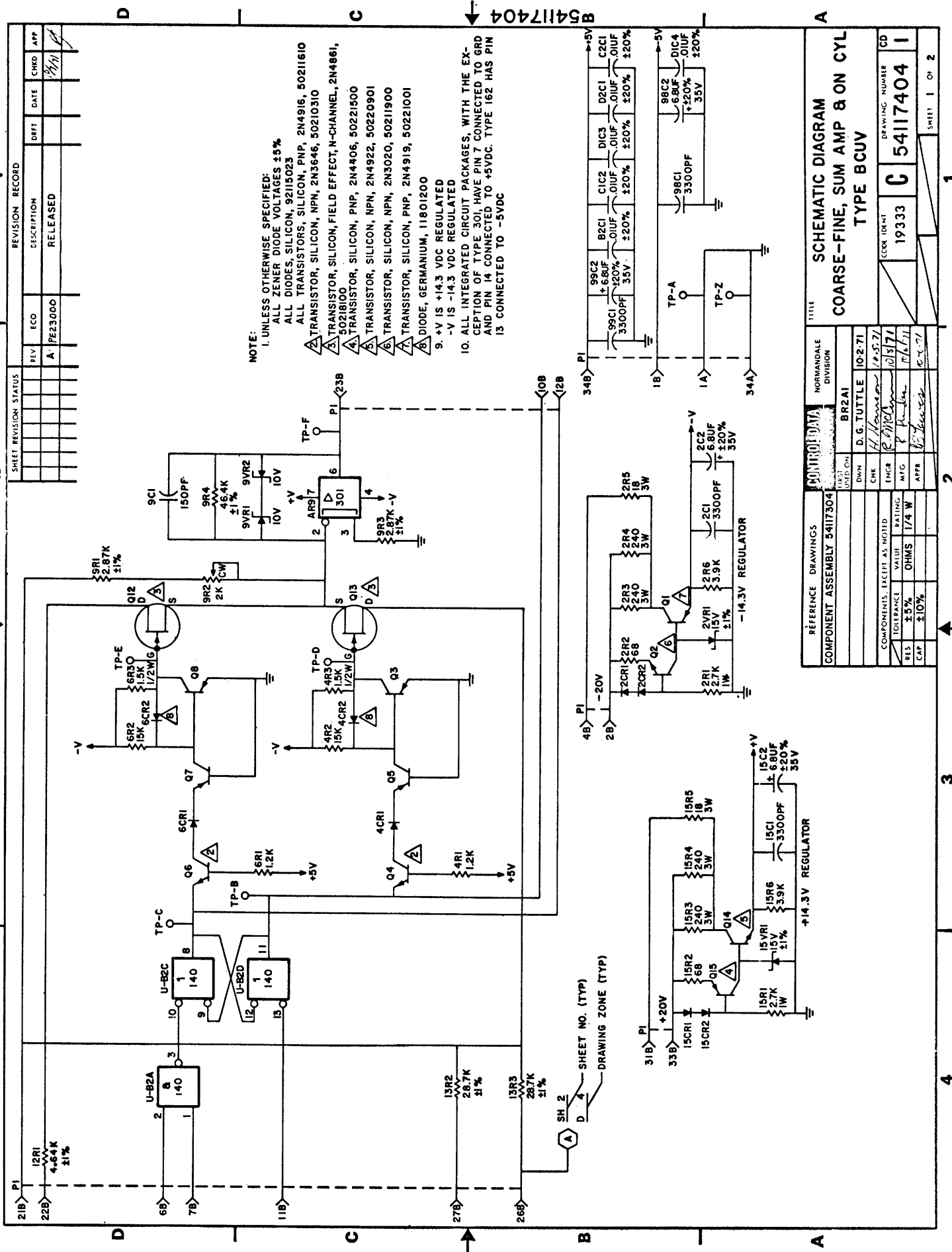


SCHEMATIC DIAGRAM
VEL 8 DESIRED VEL FUNCTION
TYPE BCTV

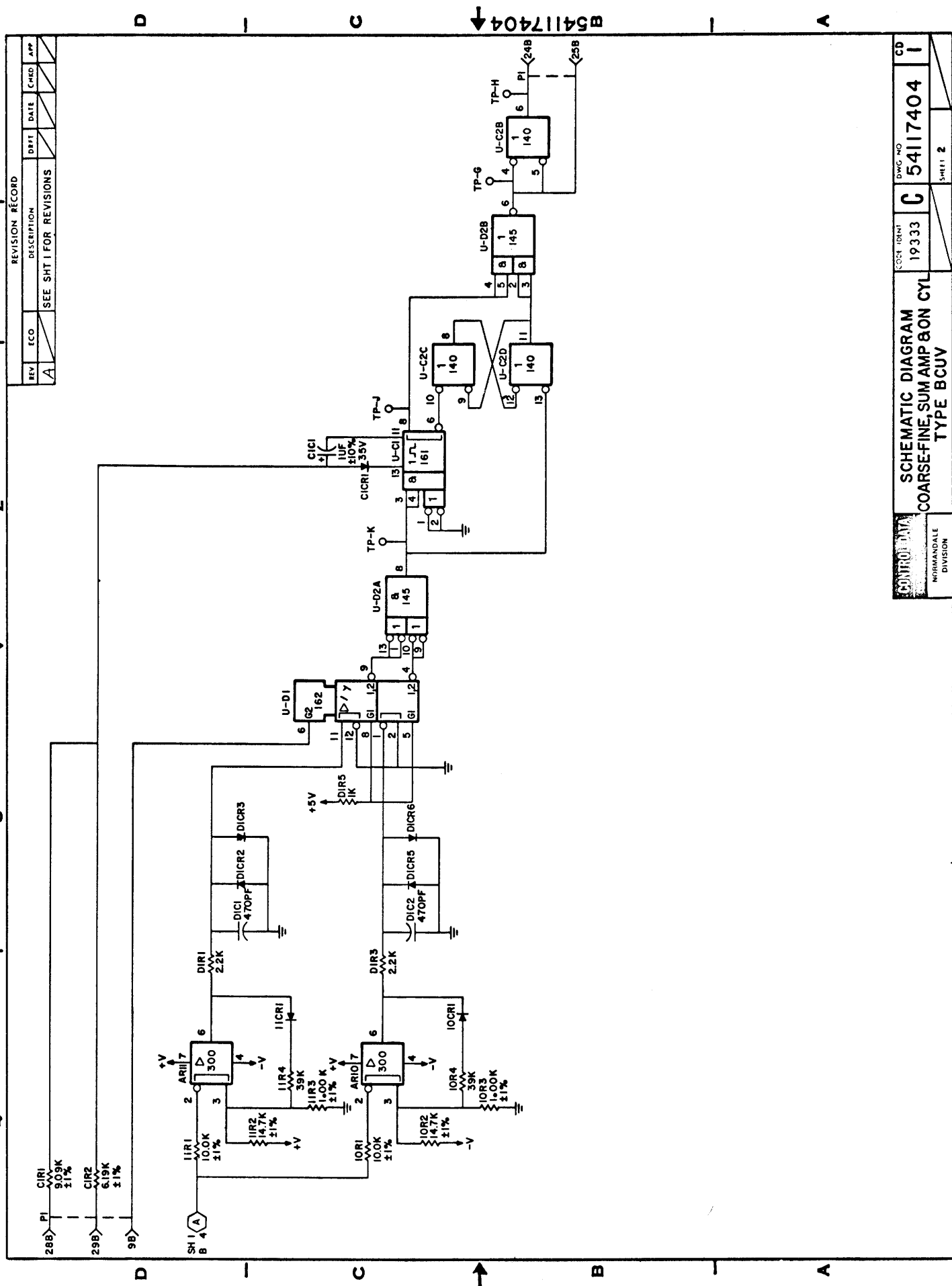
CODE IDENT 19333
C 54117002
SHEET 2



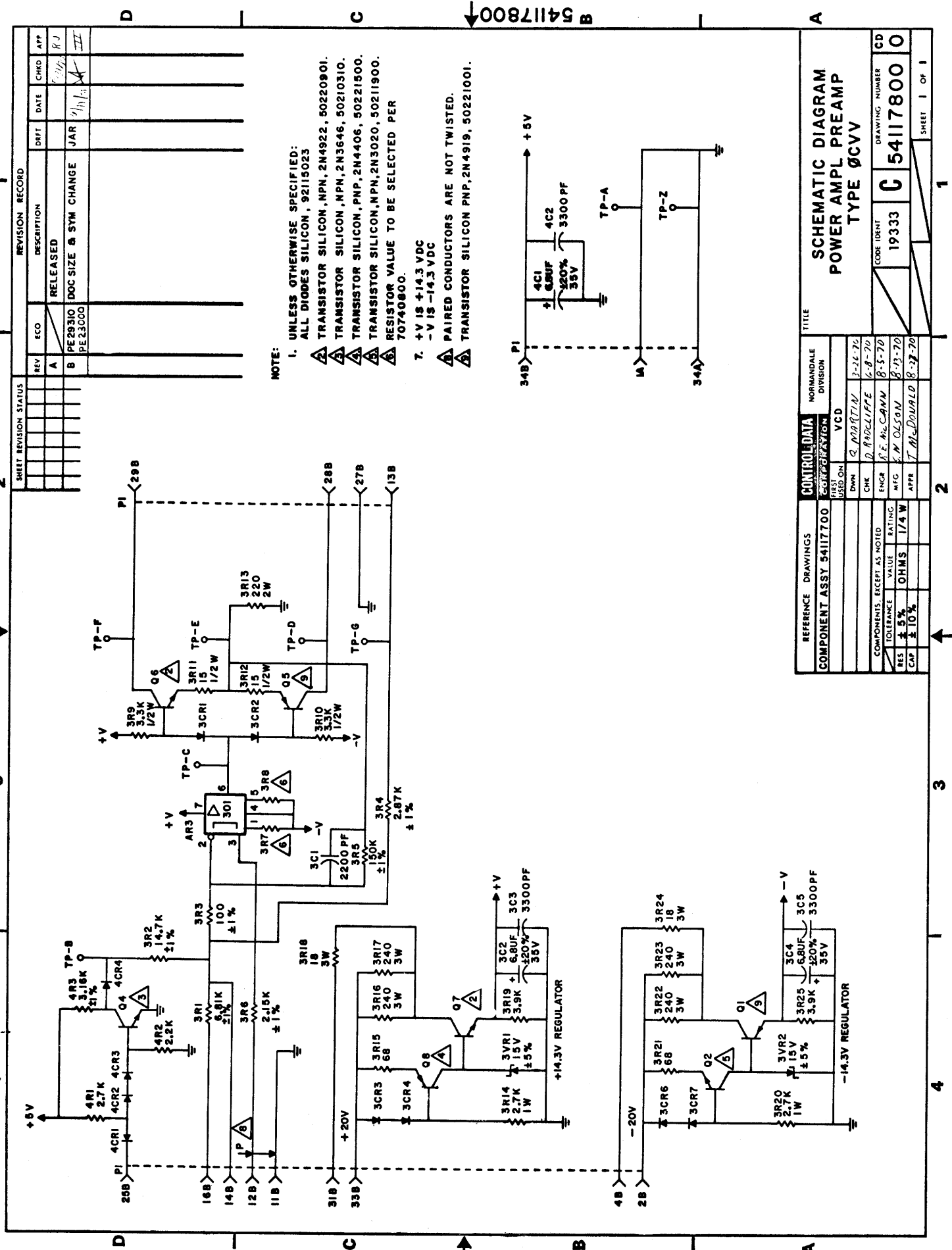




REVISION RECORD				
REV	ECO	DESCRIPTION	DATE	CHKD
A		SEE SHT 1 FOR REVISIONS		



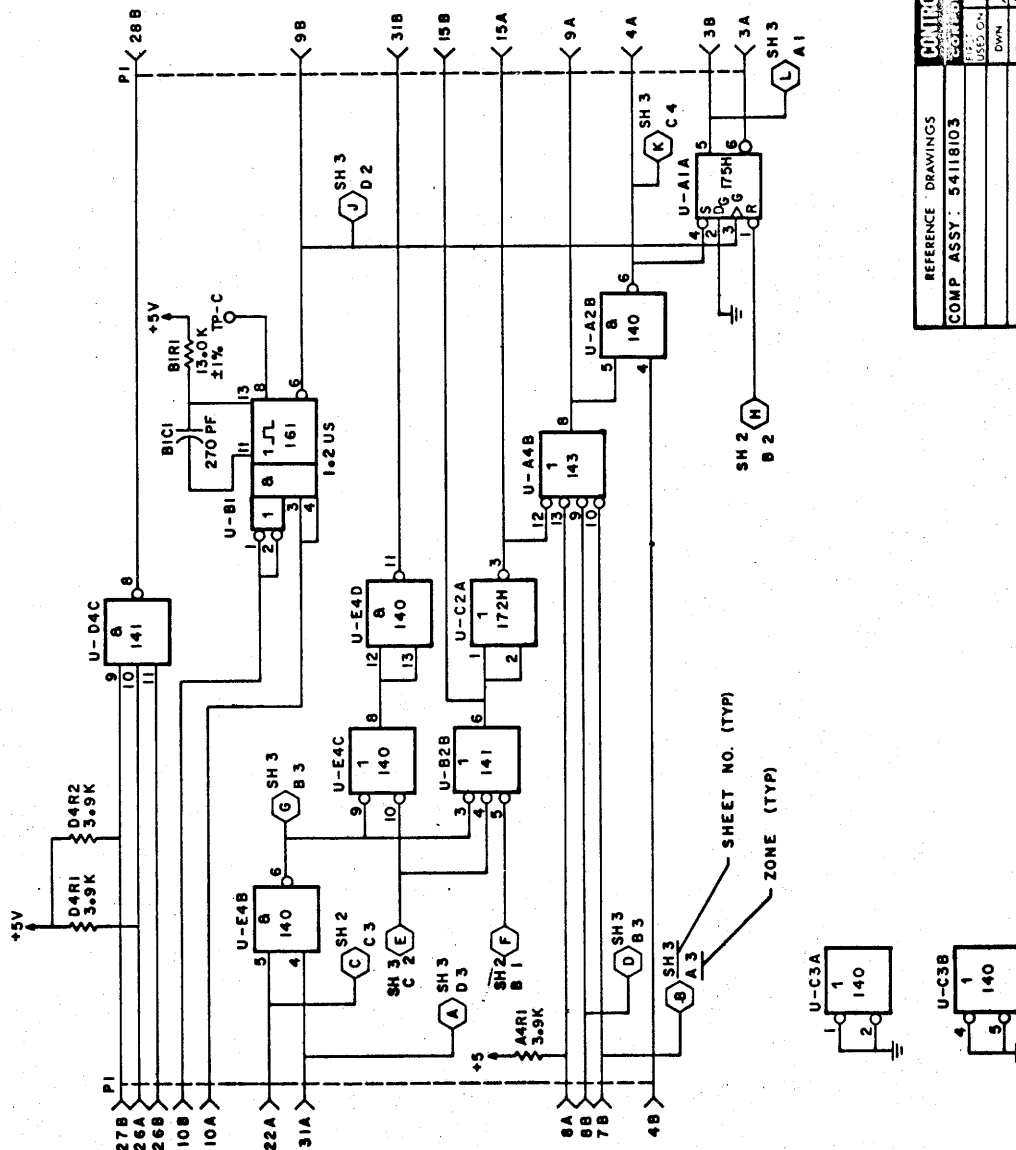
CONTROL DATA		SCHEMATIC DIAGRAM		DWG NO		CD	
NORMANDALE DIVISION		COARSE-FINE, SUM AMP 80N CYL		C 54117404		1	
		TYPE BCUV		1933		Sheet 2	

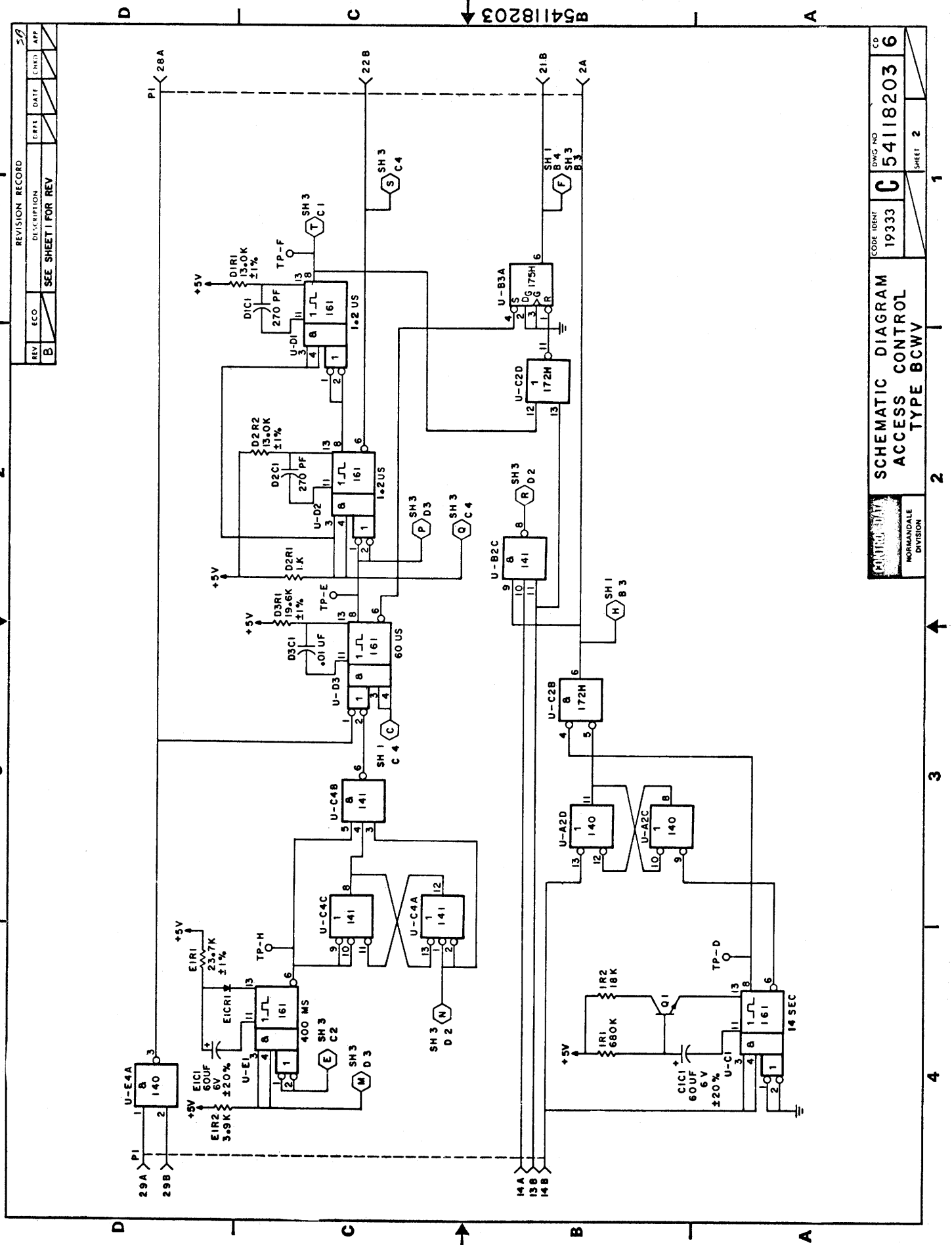


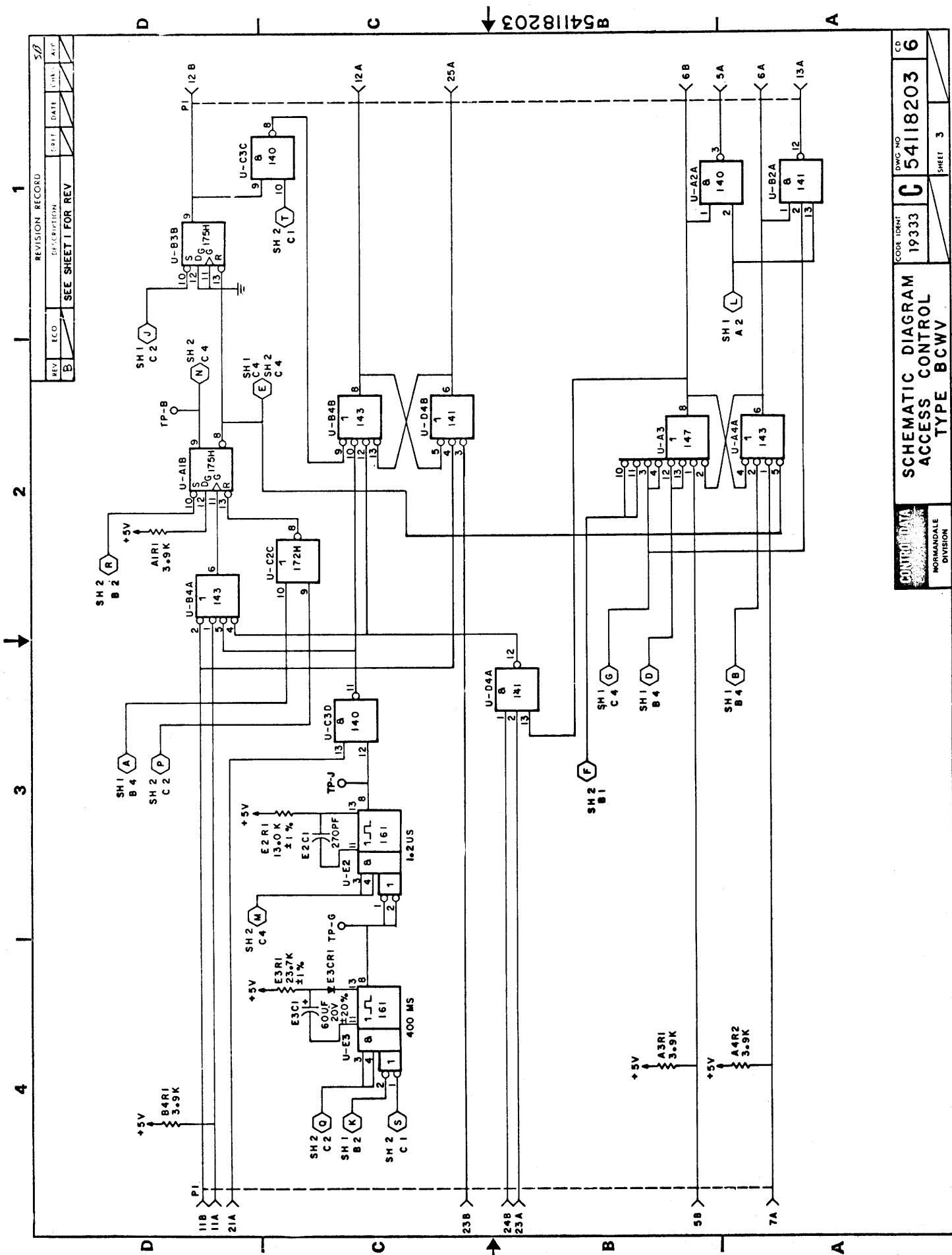
[illegible]

I. UNLESS OTHERWISE SPECIFIED:

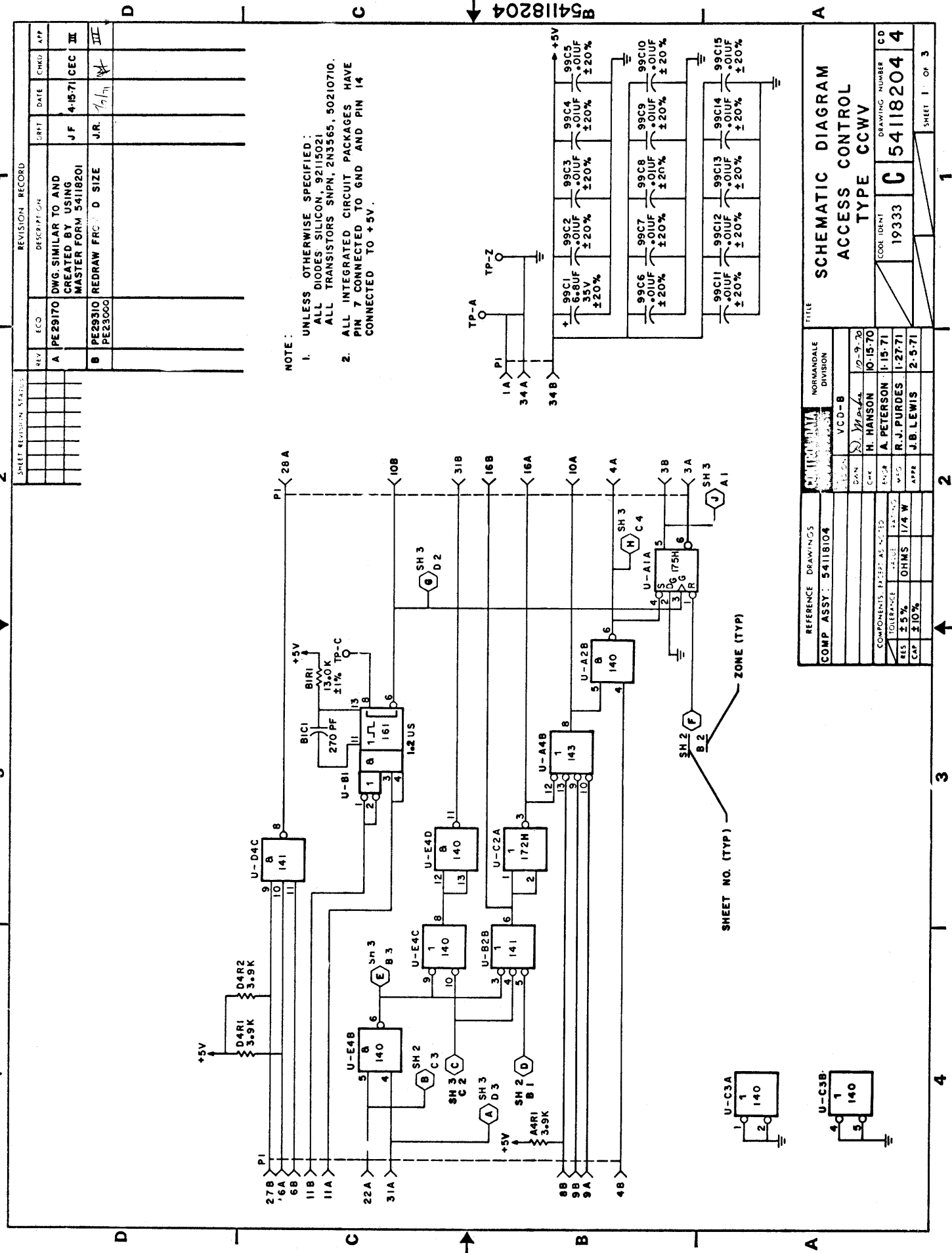
1. ALL OTHERS: 92115021
ALL DIODES SILICON, 92115021
ALL TRANSISTORS SNPN, 2N3365, 50210710.
2. ALL INTEGRATED CIRCUIT PACKAGES HAVE
PIN 7 CONNECTED TO GND AND PIN 14
CONNECTED TO +5V.

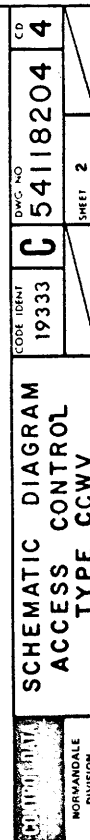
[illegible]

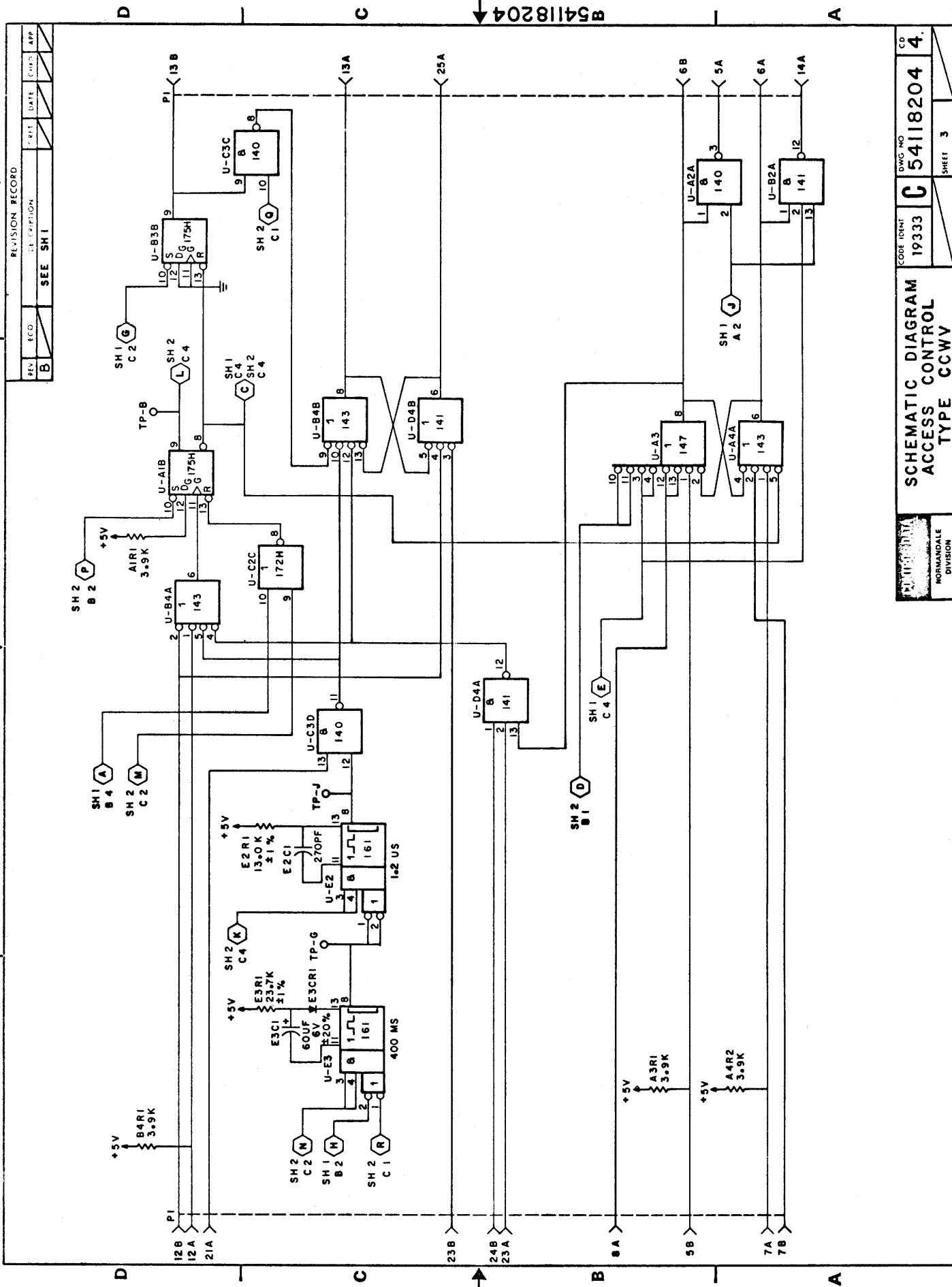




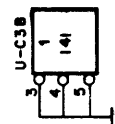
B54118203





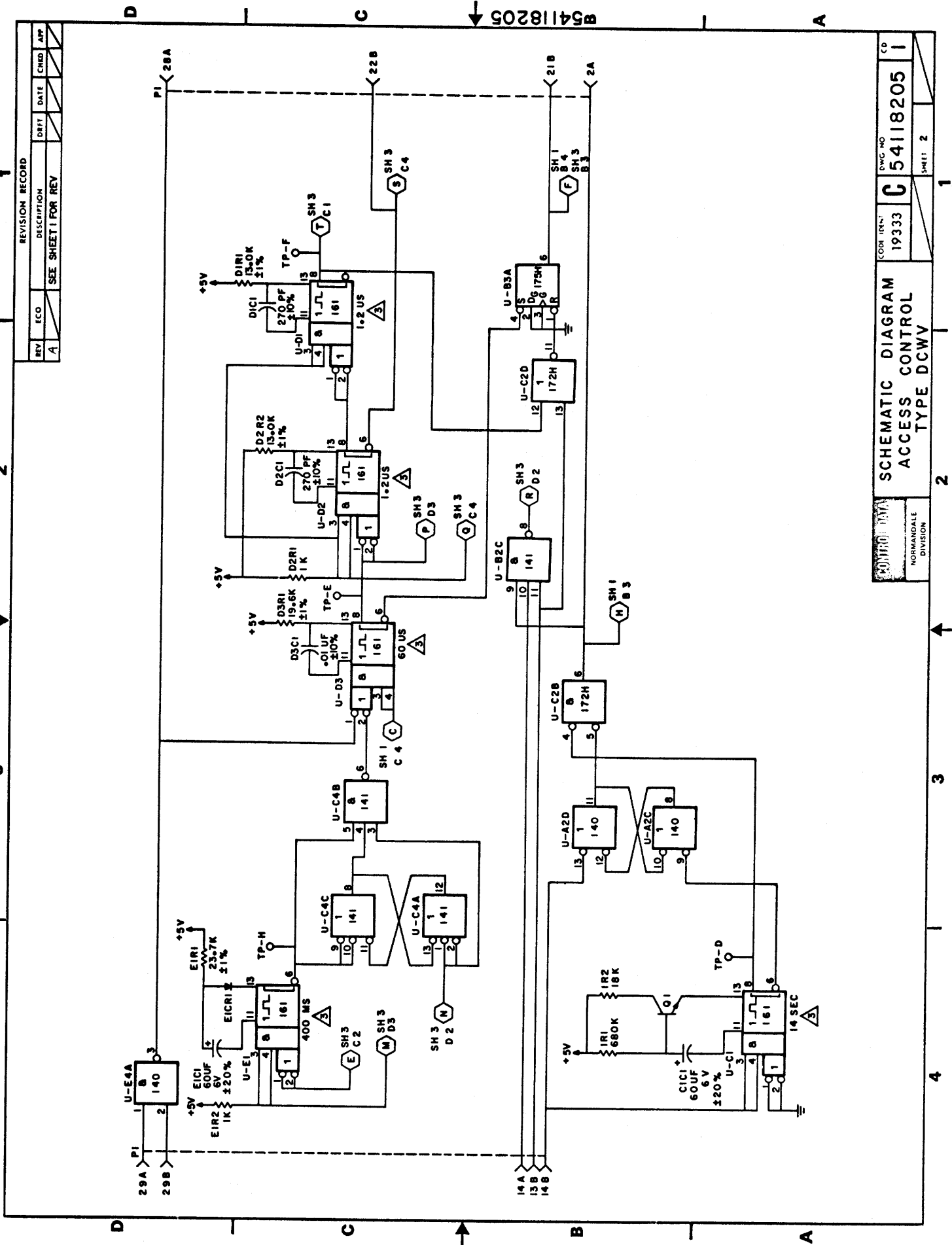


SCHEMATIC DIAGRAM		CODE IDENT	DWG NO	CD
ACCESS CONTROL		19333	C 54118204	4.
TYPE CCWV			SHEET 3	
NORMANDALE DIVISION				

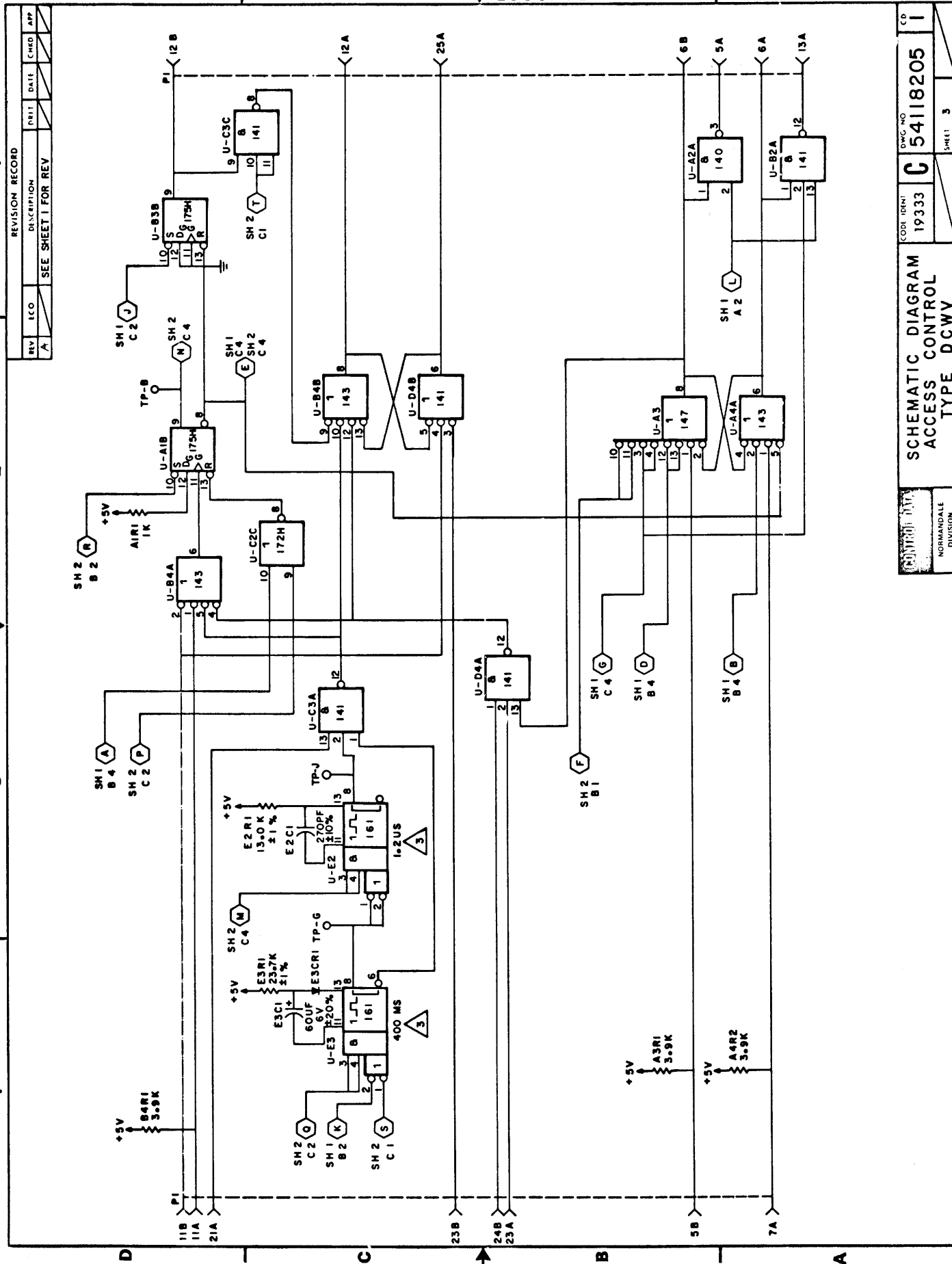


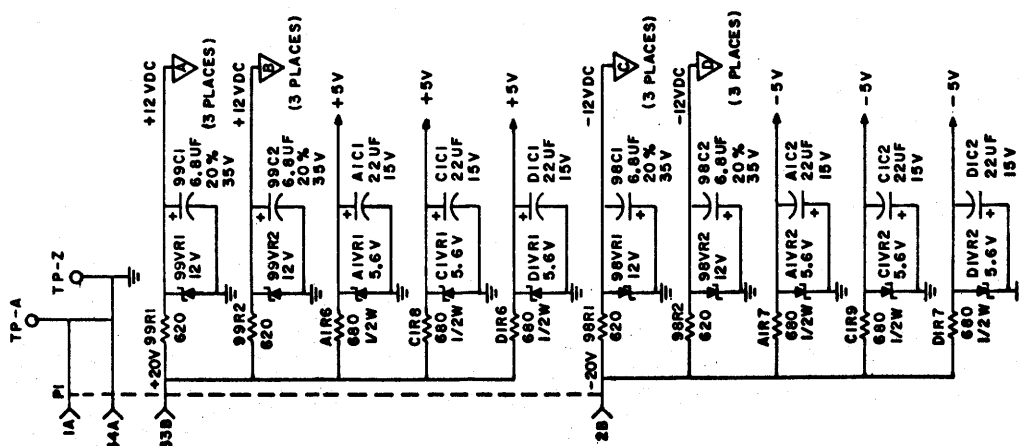
REFERENCE	DRAWINGS	COMP ASSY: 54118105		TITLE	
		CONTROL DATA		SCHEMATIC DIAGRAM	
		NORMANDALE DIVISION		ACCESS CONTROL	
		BR2A5B		TYPE DCWV	
		UNIT ON	OWN	9-3-71	
			CHK	9-3-71	
			ENGR	9-3-71	
			MTC	9-3-71	
			APP	9-3-71	
		COMPONENTS EXCEPT AS NOTED			
	TOLERANCE	VALUE	RATING		
RES	$\pm 5\%$	OHMS	1/4 W		
CAP	-30%				
			CD	54118205	1
			19333	0	
			CONC	10M	
			URBAN INC.	NUMBER	
			SHEET 1 OF 3		

1. UNLESS OTHERWISE SPECIFIED:
ALL DIODES SILICON, 92115021
ALL TRANSISTORS SNPN, 2N3565, 50210710.
2. ALL INTEGRATED CIRCUIT PACKAGES HAVE
PIN 7 CONNECTED TO GND AND PIN 14
CONNECTED TO +5V.
3. DELAY TIME FOR REFERENCE ONLY



B54118205





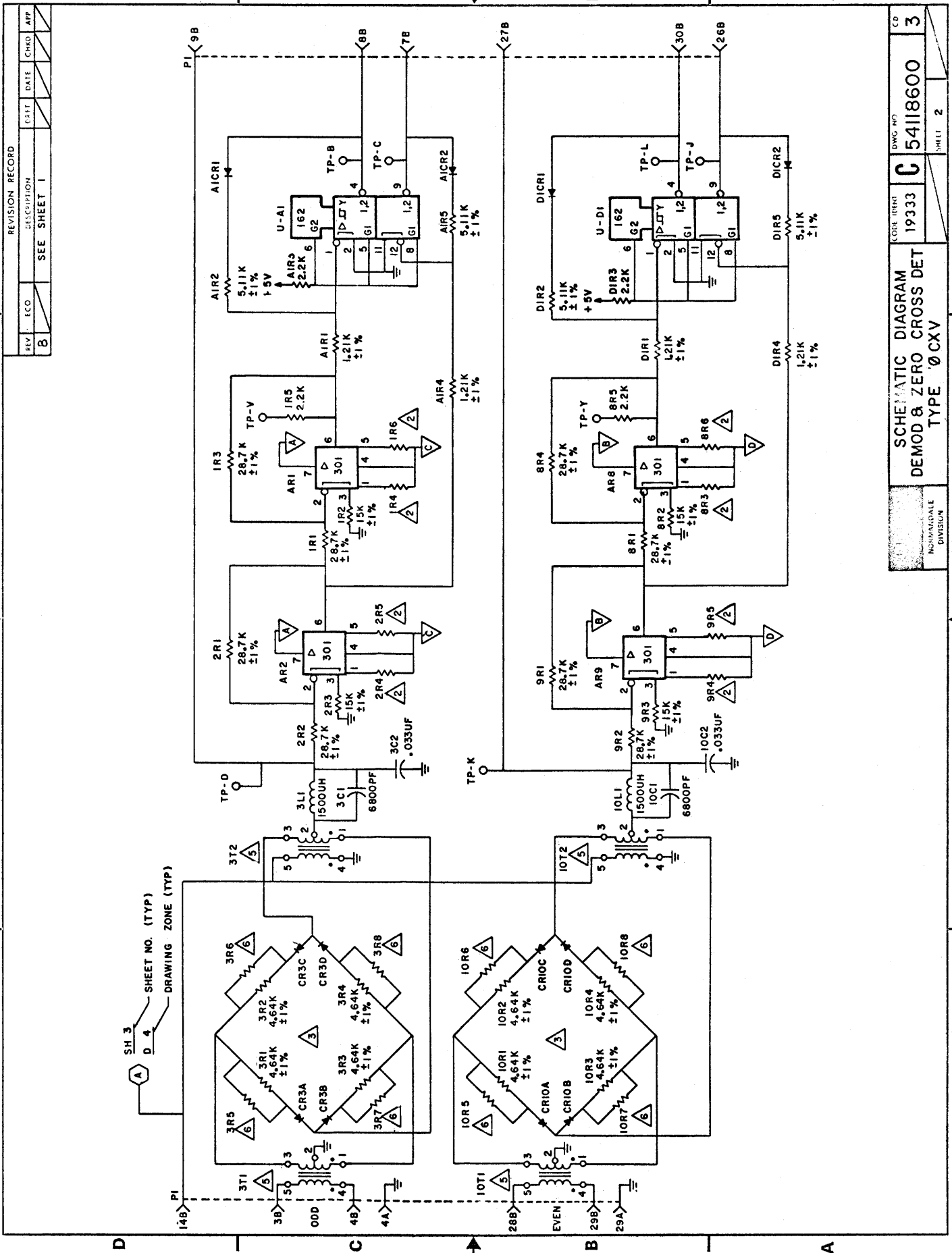
NOTE:

1. UNLESS OTHERWISE SPECIFIED
ALL DIODES, SILICON, 92118023
ALL INDUCTOR VALUES $\pm 10\%$
ALL ZENER VOLTAGES $\pm 5\%$
2. RESISTOR VALUE DETERMINED PER 70740800.
3. DIODE, QUAD-MATCHED, 50240800
4. ALL INTEGRATED CIRCUITS, WITH THE EXCEPTION OF TYPE 301, HAVE PIN 7 CONNECTED TO GND, PIN 14 CONNECTED TO +5VDC, AND PIN 13 CONNECTED TO -5VDC
5. TRANSFORMER, 94245916
6. SEE 0CXV RECOMMENDED TEST PROCEDURE 54118700

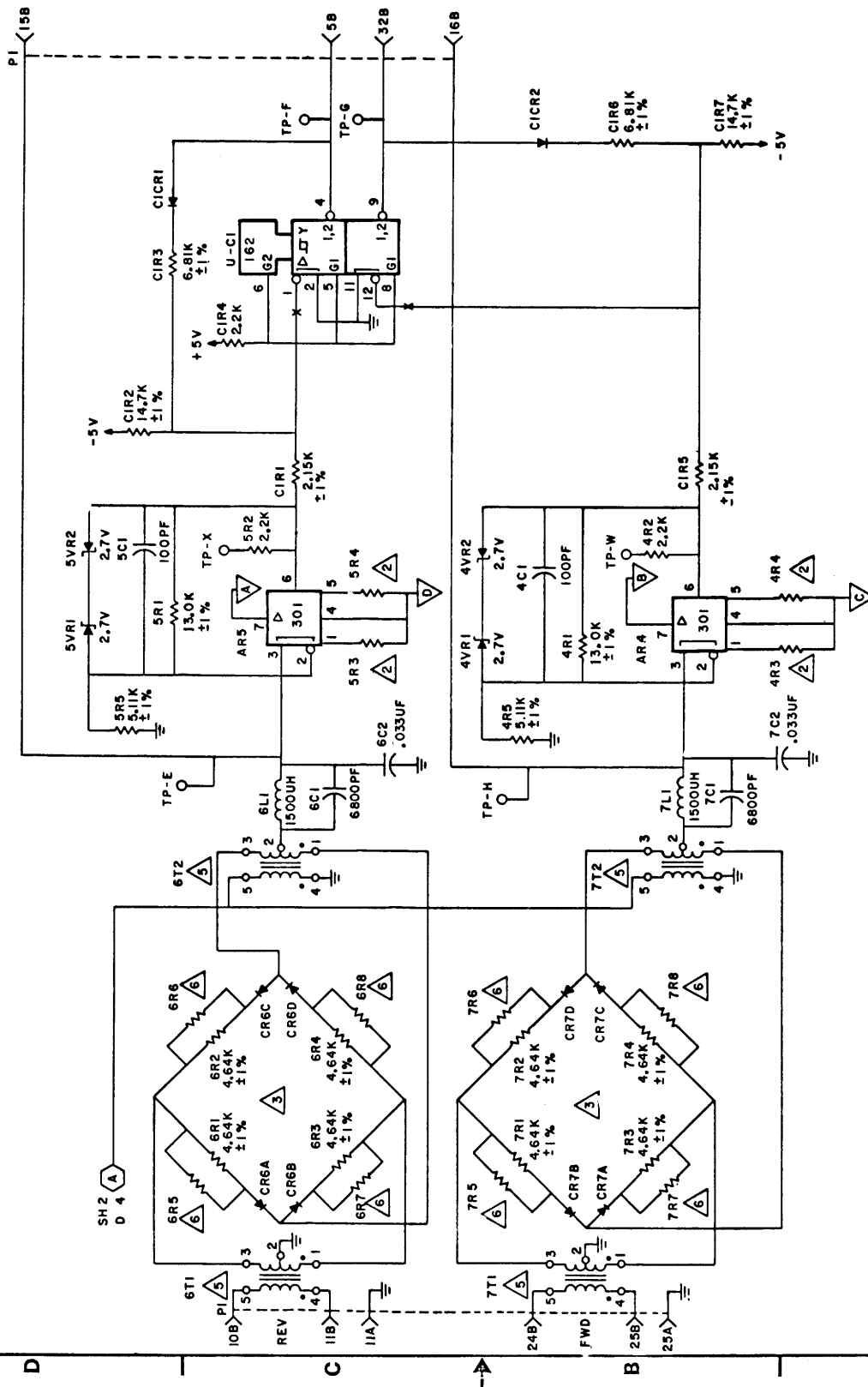
SHEET REVISION STATUS					REVISION RECORD				
REV	ECO	DESCRIPTION			DATE	CHKD	APP		
A		RELEASE							
B		DOC SIZE & SYM CHANGE			JAR 6/17/71	✓	✓		
		PE2300							
		PE23000							

[illegible]

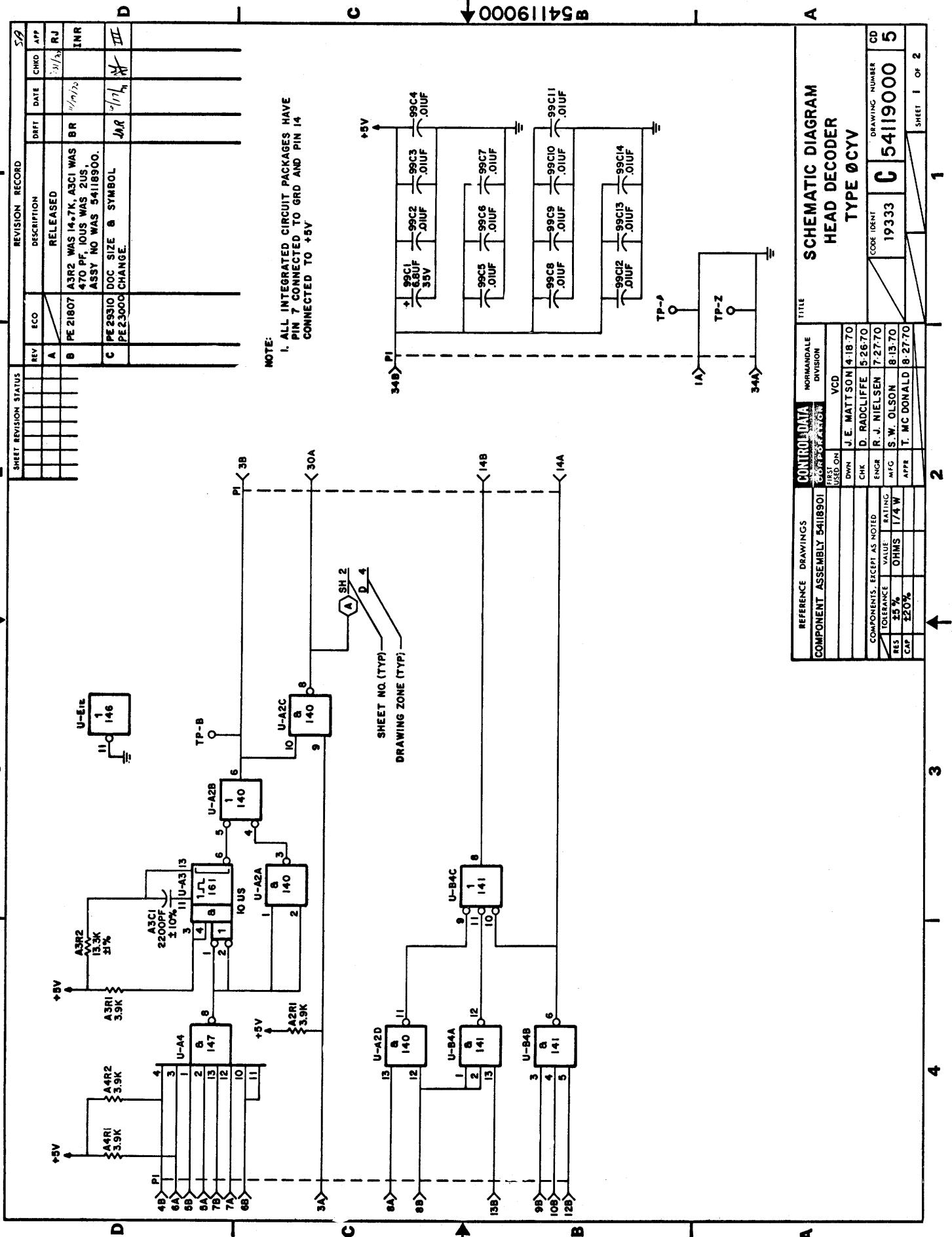




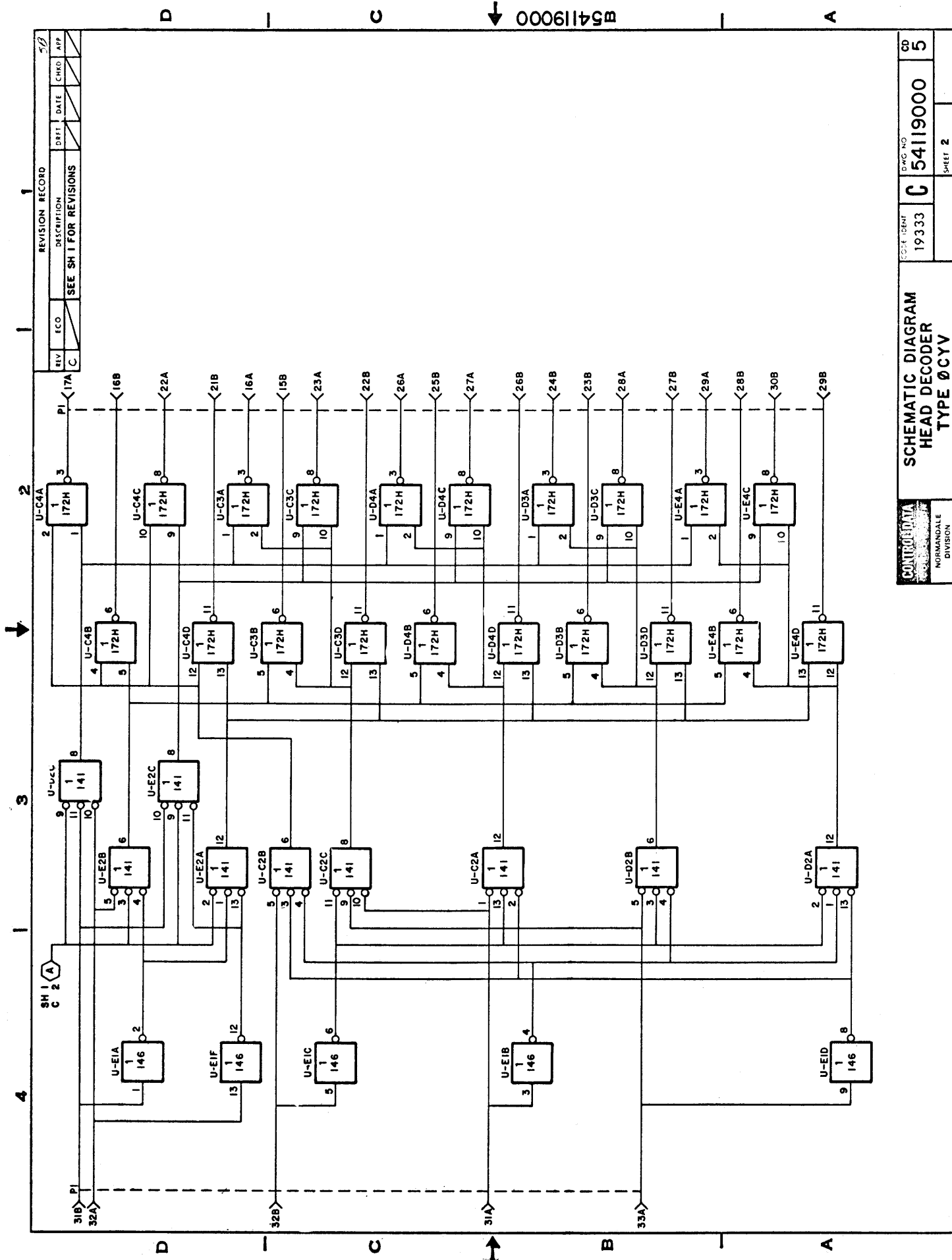
REVISION RECORD			
REV	ECO	DESCRIPTION	DATE
B		SEE SHEET 1	
		CHKD	APP



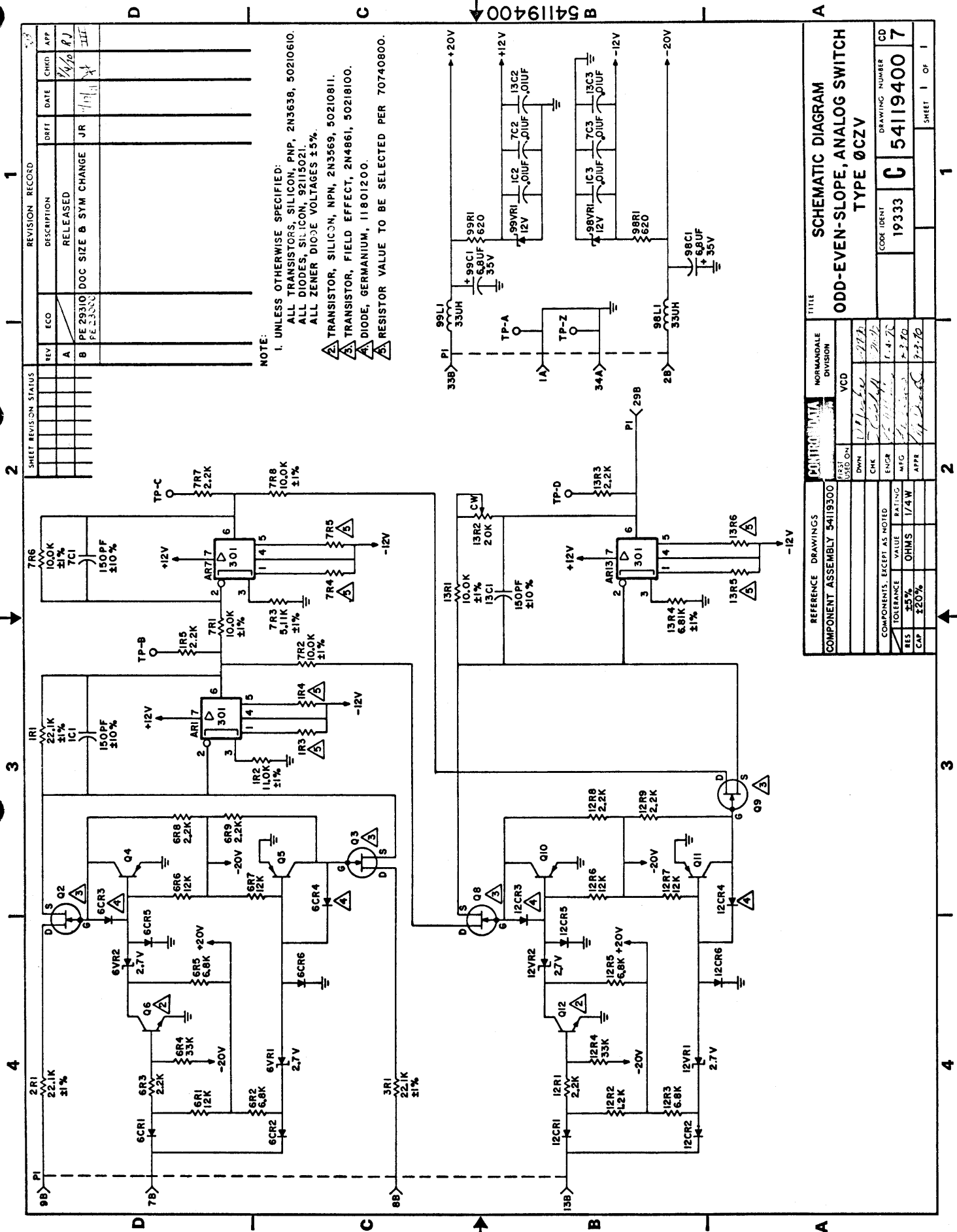
SCHEMATIC DIAGRAM			
CODE IDENT	DWG NO	SHEET	CD
19333	C	54118600	3
DEMOM 8 ZERO CROSS DET			
TYPE ØCXV			
NORMANDALE DIVISION			



B 54119000



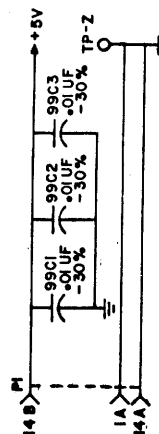
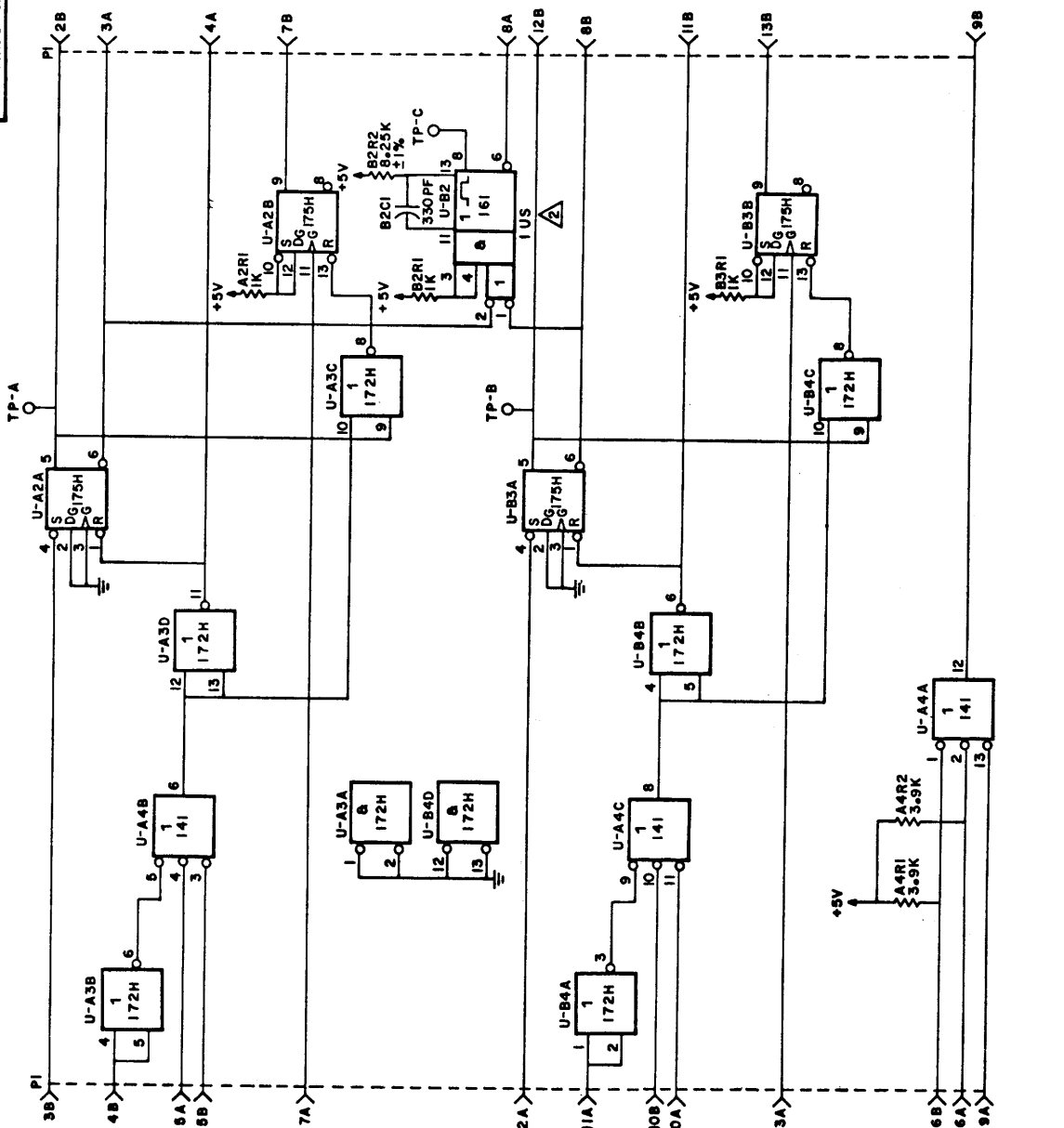
B54119000



REVISION RECORD				
REV	ECO	DESCRIPTION	DATE	CHKD APP
A	PE23000	RELEASED		5/19/72 <i>[Signature]</i>

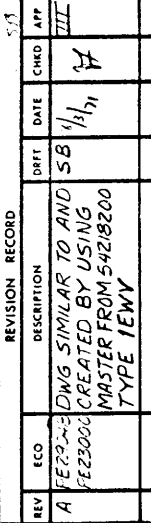
NOTE:

1. ALL IC PACKAGES HAVE PIN 7 CONNECTED TO GND AND PIN 14 CONNECTED TO +5V.
2. FOR REFERENCE ONLY



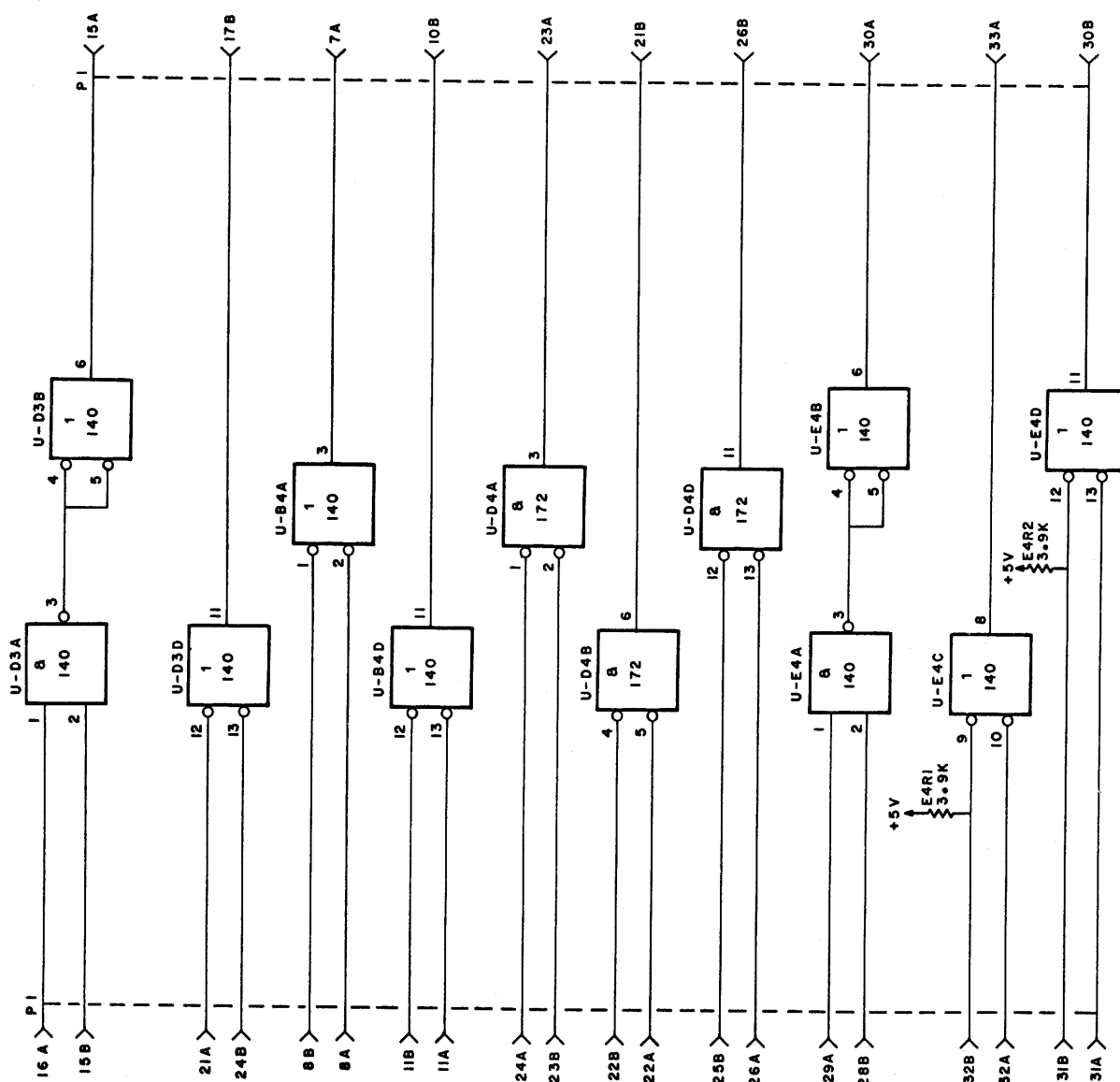
REFERENCE DRAWINGS		COMPONENT ASSY 54211700		CONTROL DATA CORPORATION FIRST USED ON BRZA4		NORMANDALE DIVISION TITLE SCHEMATIC DIAGRAM UNIT RESERVE TYPE 1EEV		CD DRAWING NUMBER 54211800		CODE IDENT 19333		SHEET 1 OF 1	
COMPONENTS, EXCEPT AS NOTED				DWN Q. MARTIN 7/27/71		CHK [Signature] 8-3-71		ENGR [Signature] 8-11-71		MFG [Signature] 8-12-71		APPR [Signature] 8-17-71	
TOLERANCE		VALUE		RATING									
RES $\pm 5\%$		OHMS		1/W									
CAP $\pm 10\%$													





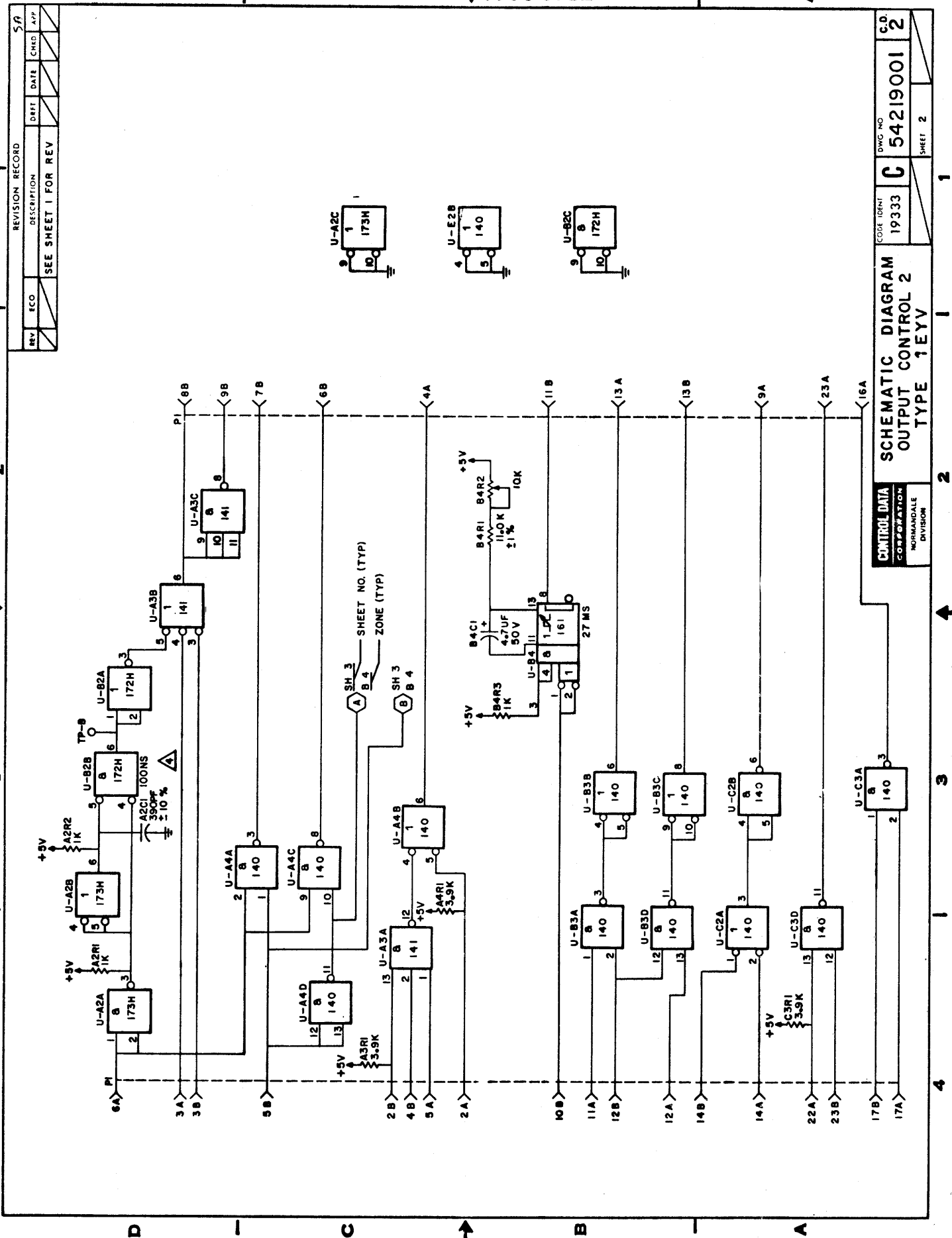
CONTROL DATA		SCHEMATIC DIAGRAM HOLD & DISCONNECT TYPE AEV		CD
NORMANDALE DIVISION		19333	54218201	9
		DWG NO		
		SHEET 2 OF 2		

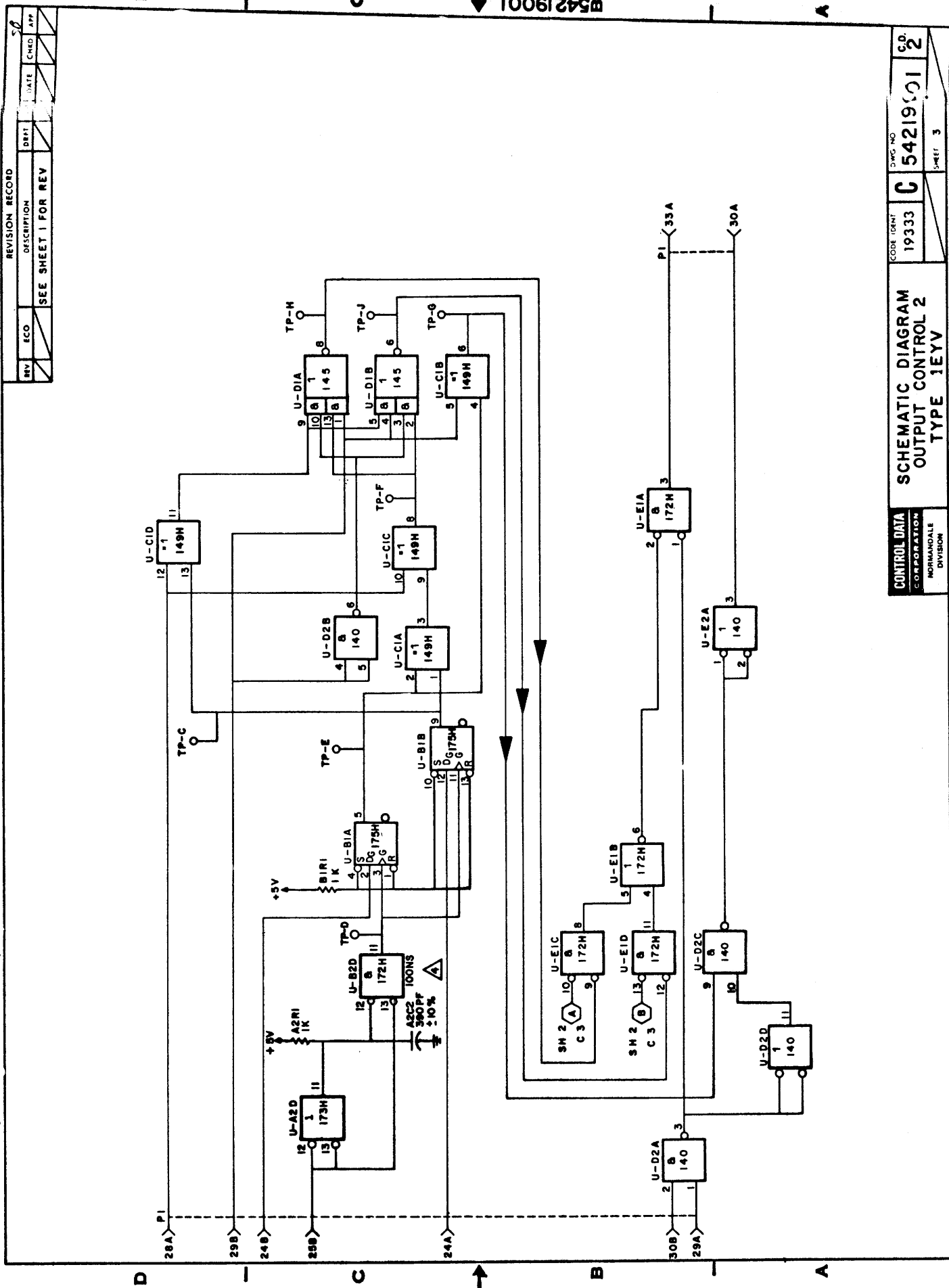
REVISION RECORD				
REV	ECO	DESCRIPTION	DATE	CHKD
SEE SHT 1 FOR REV				



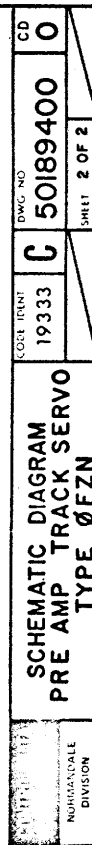
B54218201

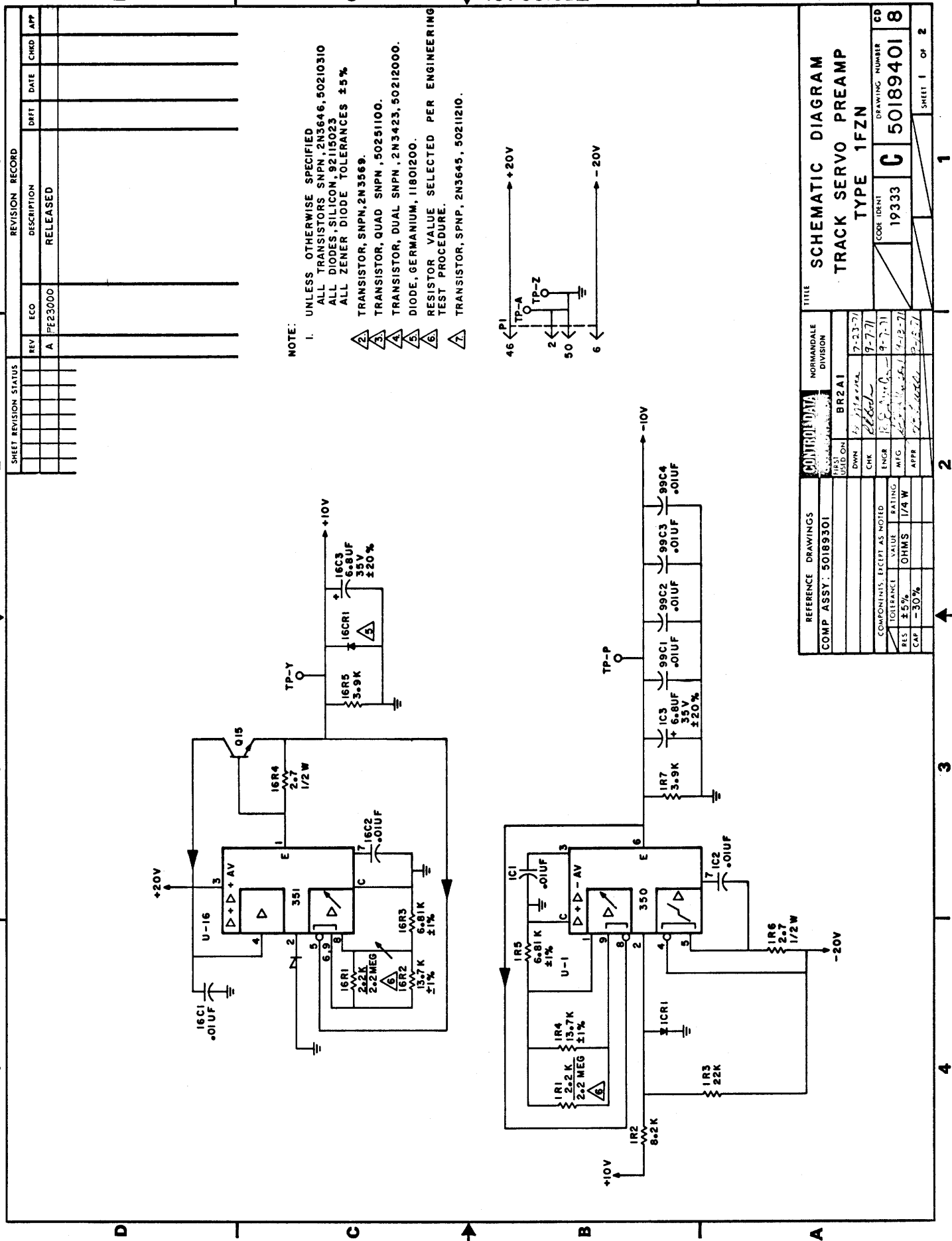






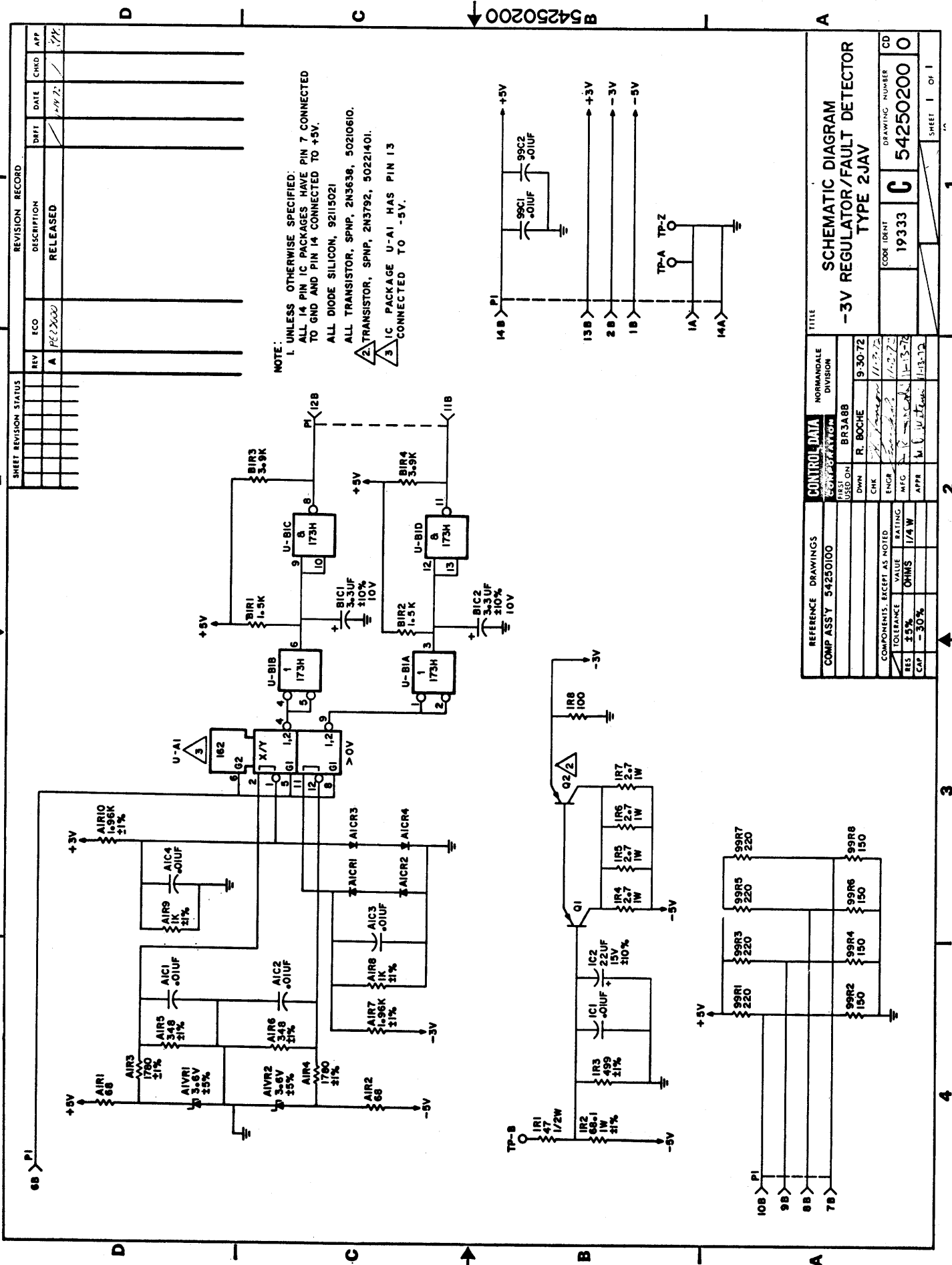
B54219001





B50189401





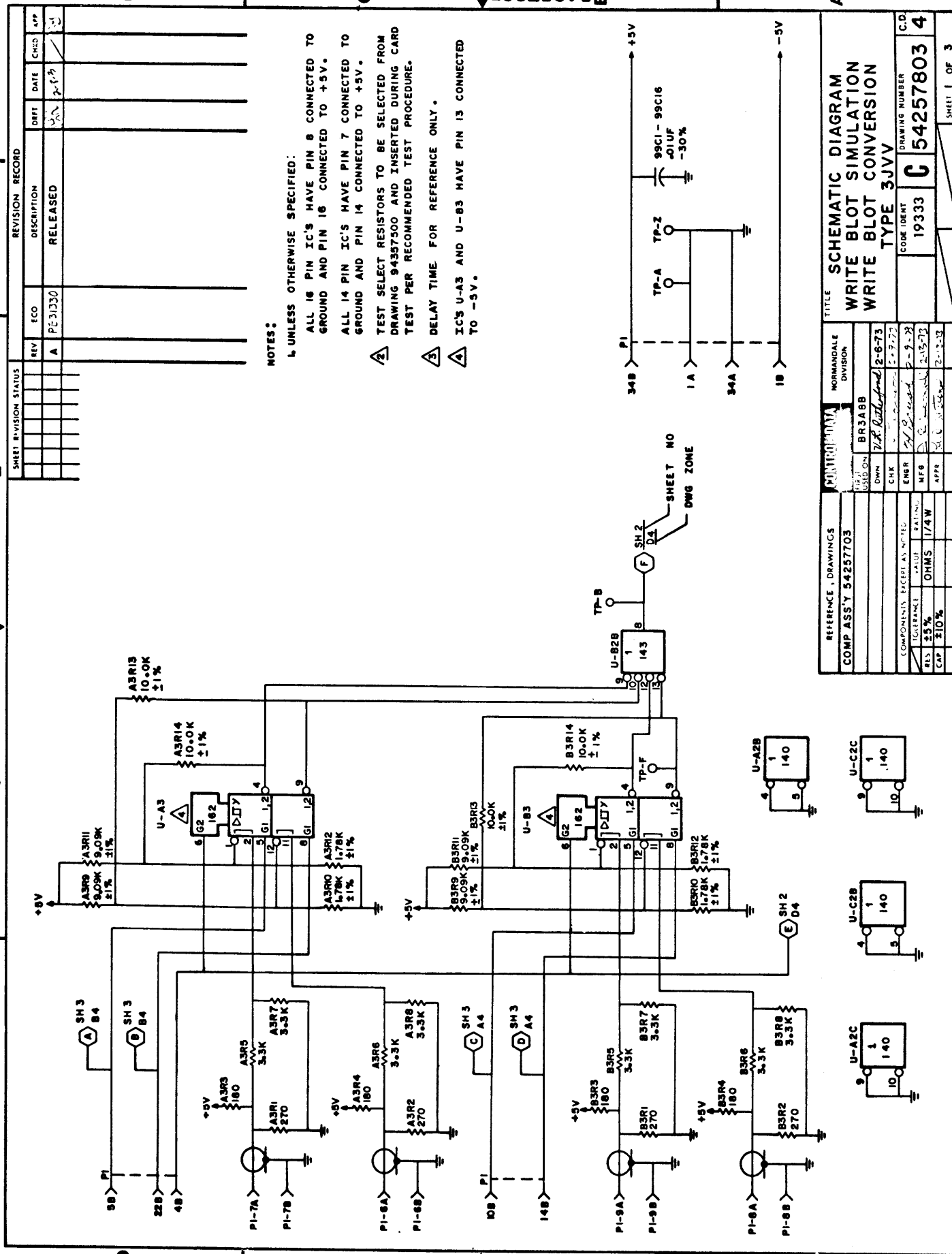
B 54250200

TITLE

SCHEMATIC DIAGRAM
-3V REGULATOR/FAULT DETECTOR
TYPE 2JAV

CD	54250200	O
DRAWING NUMBER	19333	C
CORE IDENT		

SHEET 1 OF 1



NOTES:

1. UNLESS OTHERWISE SPECIFIED:

ALL 16 PIN IC'S HAVE PIN 8 CONNECTED TO GROUND AND PIN 16 CONNECTED TO +5V.

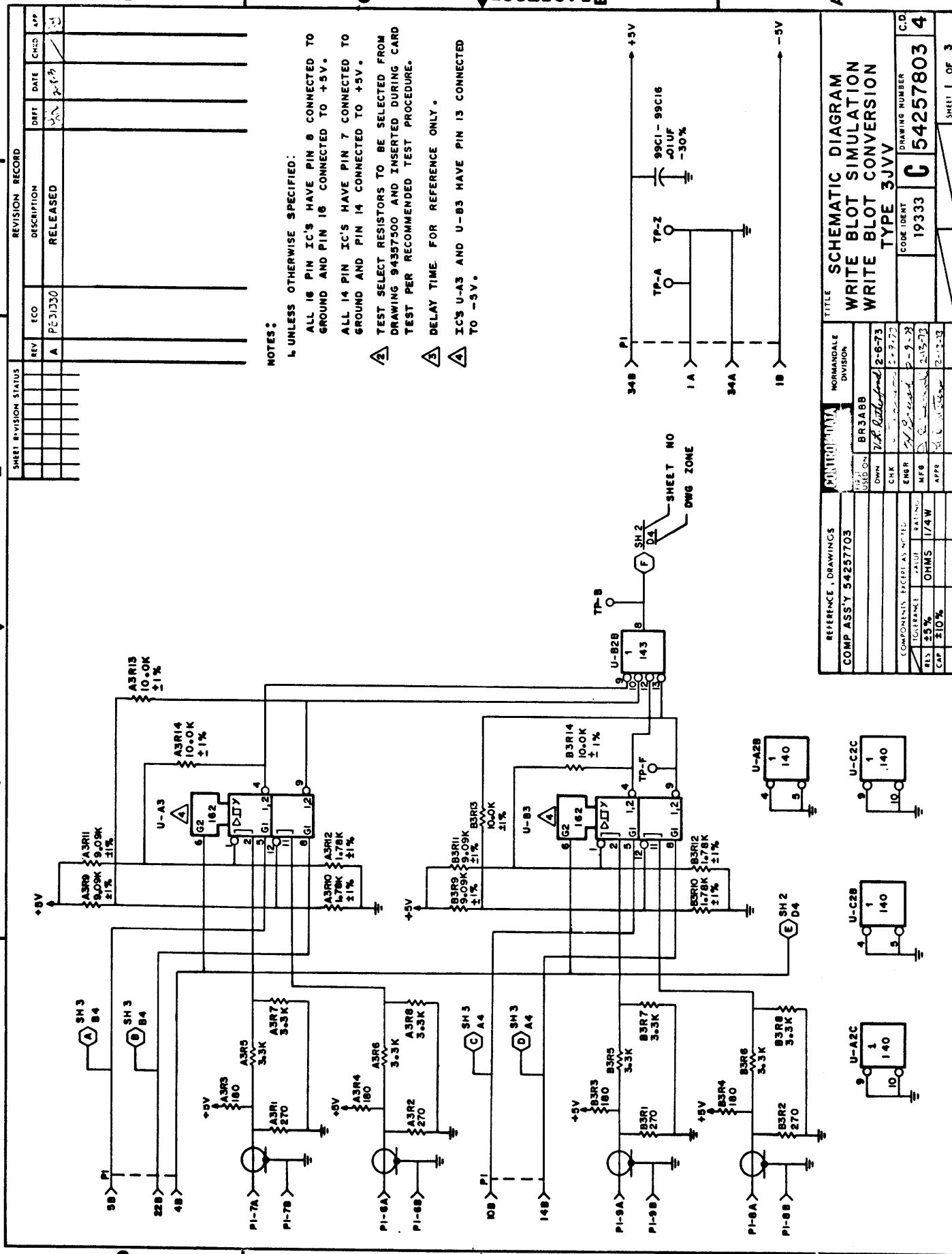
ALL 14 PIN IC'S HAVE PIN 7 CONNECTED TO GROUND AND PIN 14 CONNECTED TO +5V.

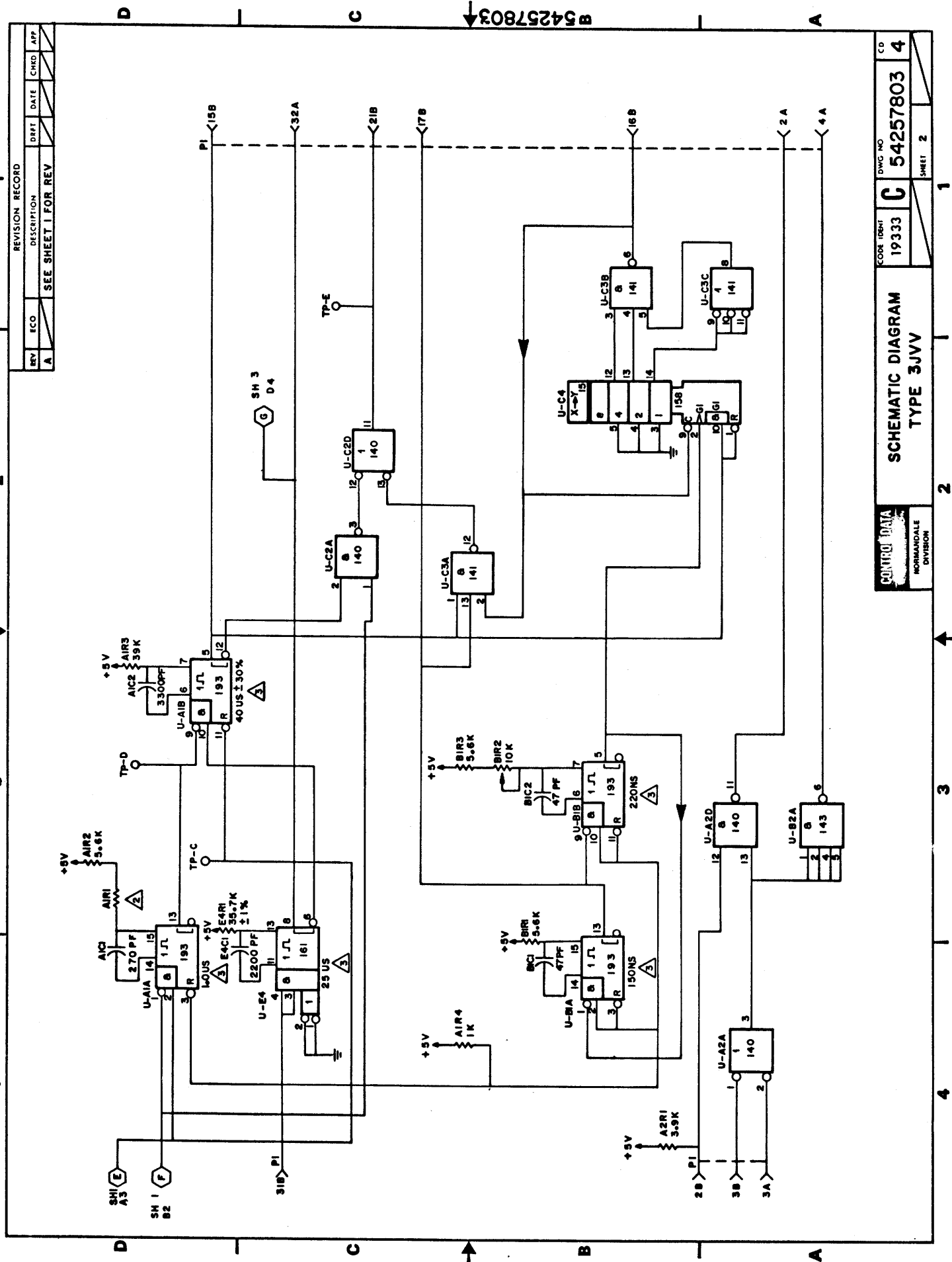
2. TEST SELECT RESISTORS TO BE SELECTED FROM DRAWING 94357500 AND INSERTED DURING CARD TEST PER RECOMMENDED TEST PROCEDURE.

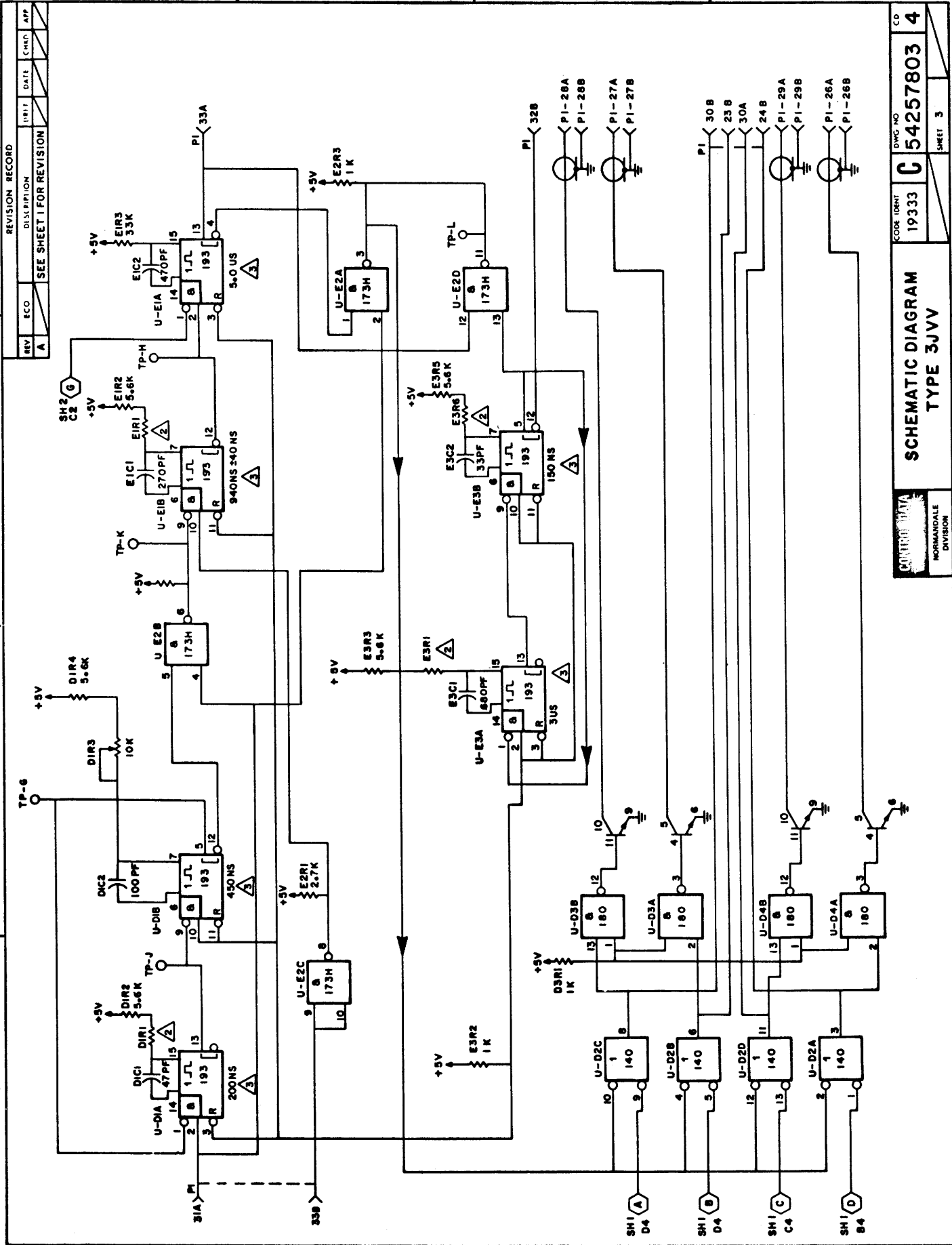
3. DELAY TIME FOR REFERENCE ONLY.

4. IC'S U-A3 AND U-B3 HAVE PIN 13 CONNECTED TO -5V.

REFERENCE, DRAWINGS		NORMANDALE DIVISION		TITLE	
COMP ASS'Y 54257703		BR3A8B		SCHEMATIC DIAGRAM	
USED ON		OWN		WRITE BLOT SIMULATION	
CHK		CHK		WRITE BLOT CONVERSION	
COMPONENTS, EXCEPT AS NOTED		CHK		TYPE 3JVV	
TOLERANCE		TOLERANCE		DRAWING NUMBER	
RES 5% ±10%		RES 5% ±10%		19333	
CAP 5% ±10%		CAP 5% ±10%		C 54257803	
APP		APP		SHEET 1 OF 3	
C.D.		C.D.		4	

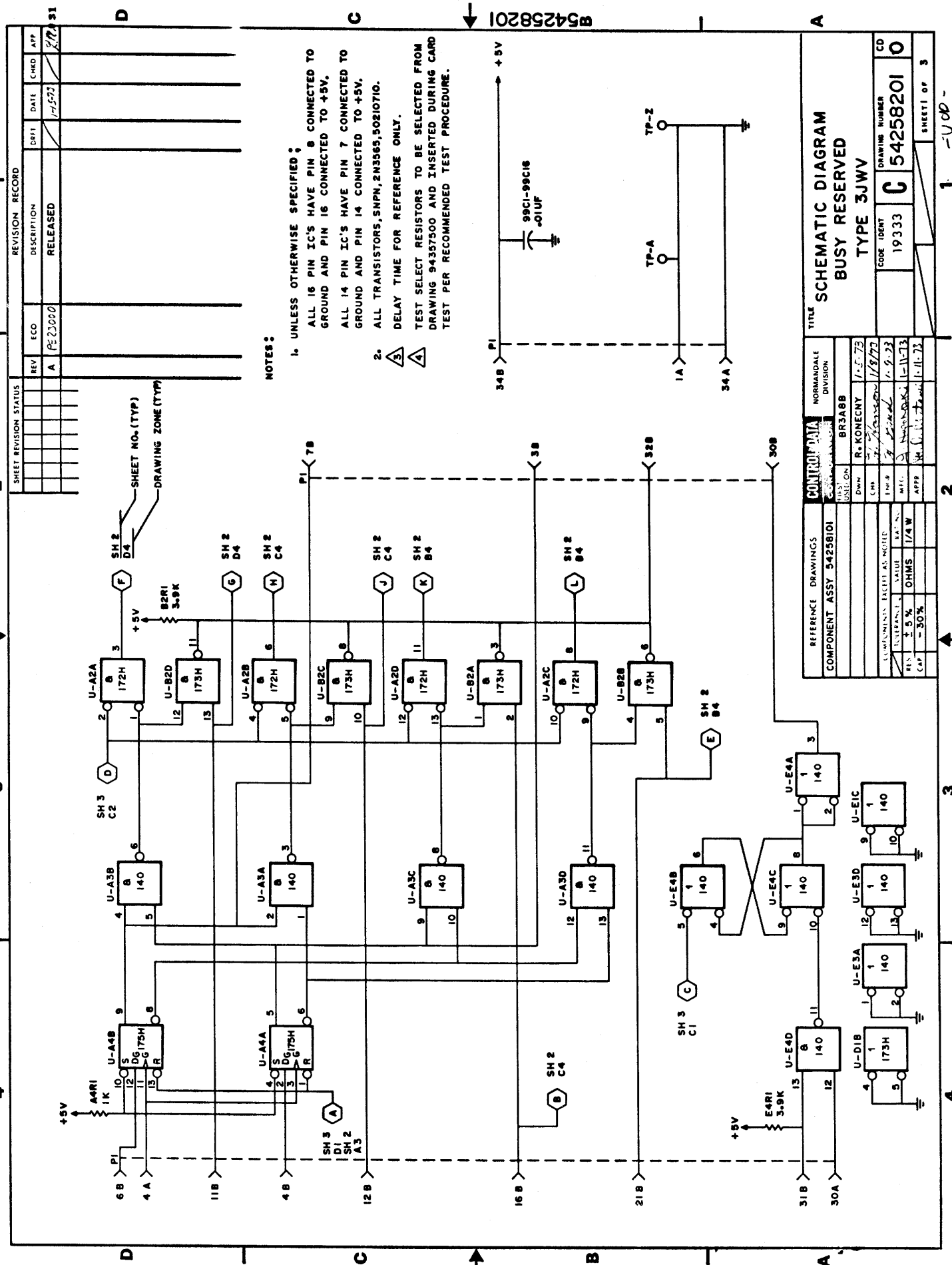




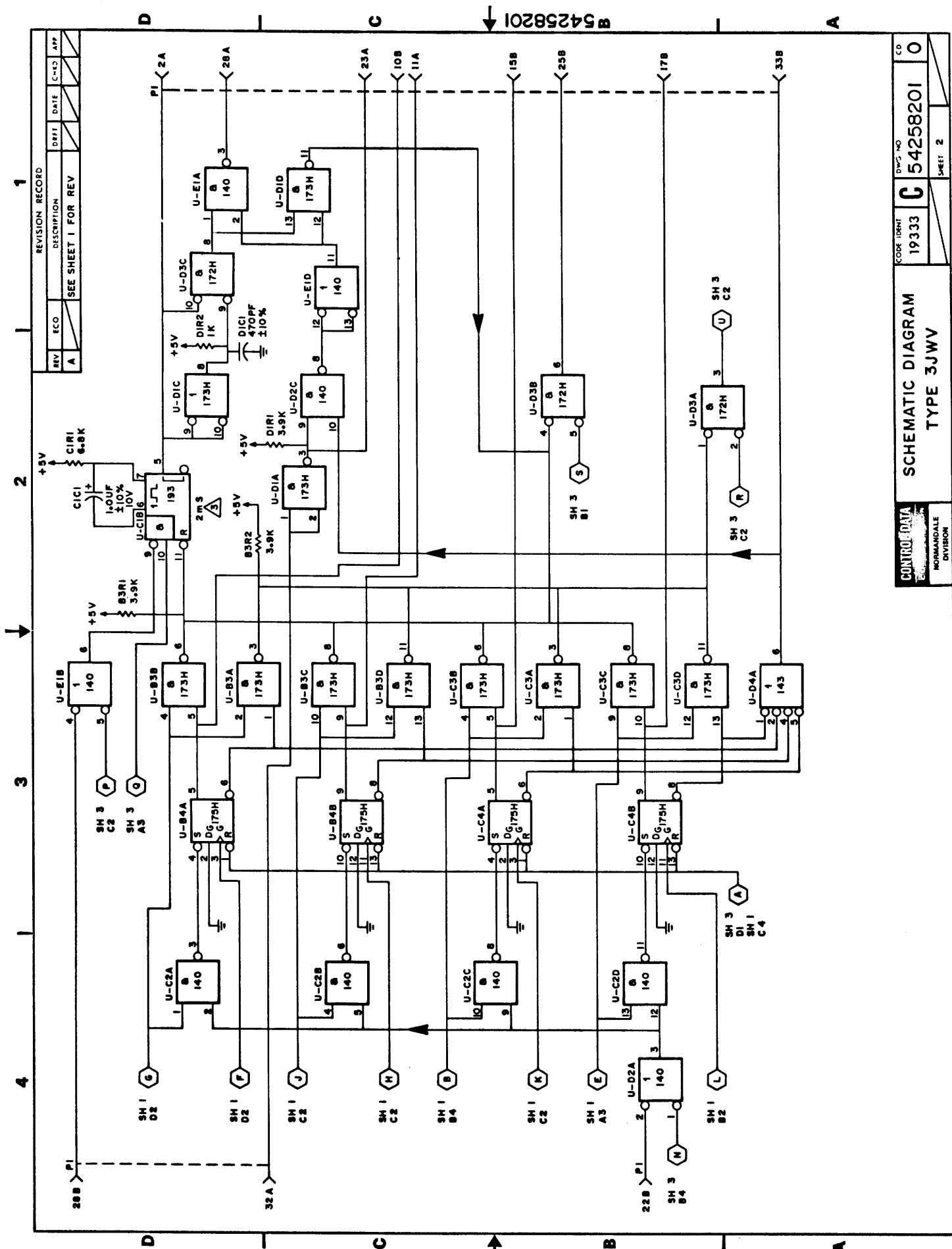


REVISION RECORD		DISPOSITION		LIBR	DATE	CHNG	APP
REV	ECO	SEE SHEET 1 FOR REVISION					
A							

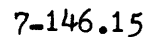
SCHEMATIC DIAGRAM		DWG NO		CD	
TYPE 3JVJ		C 54257803		4	
NORMANDALE DIVISION		19333		SHEET 3	

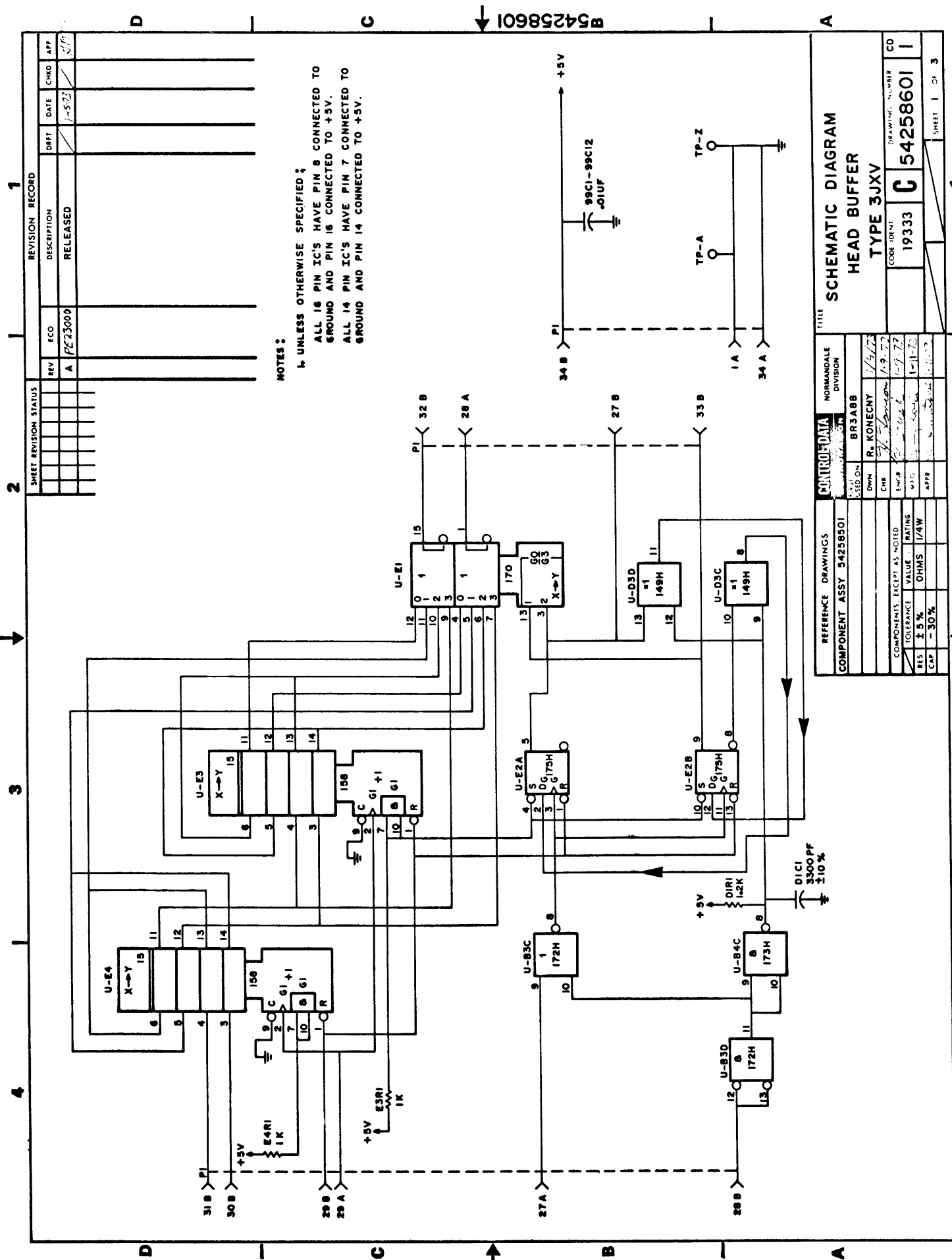


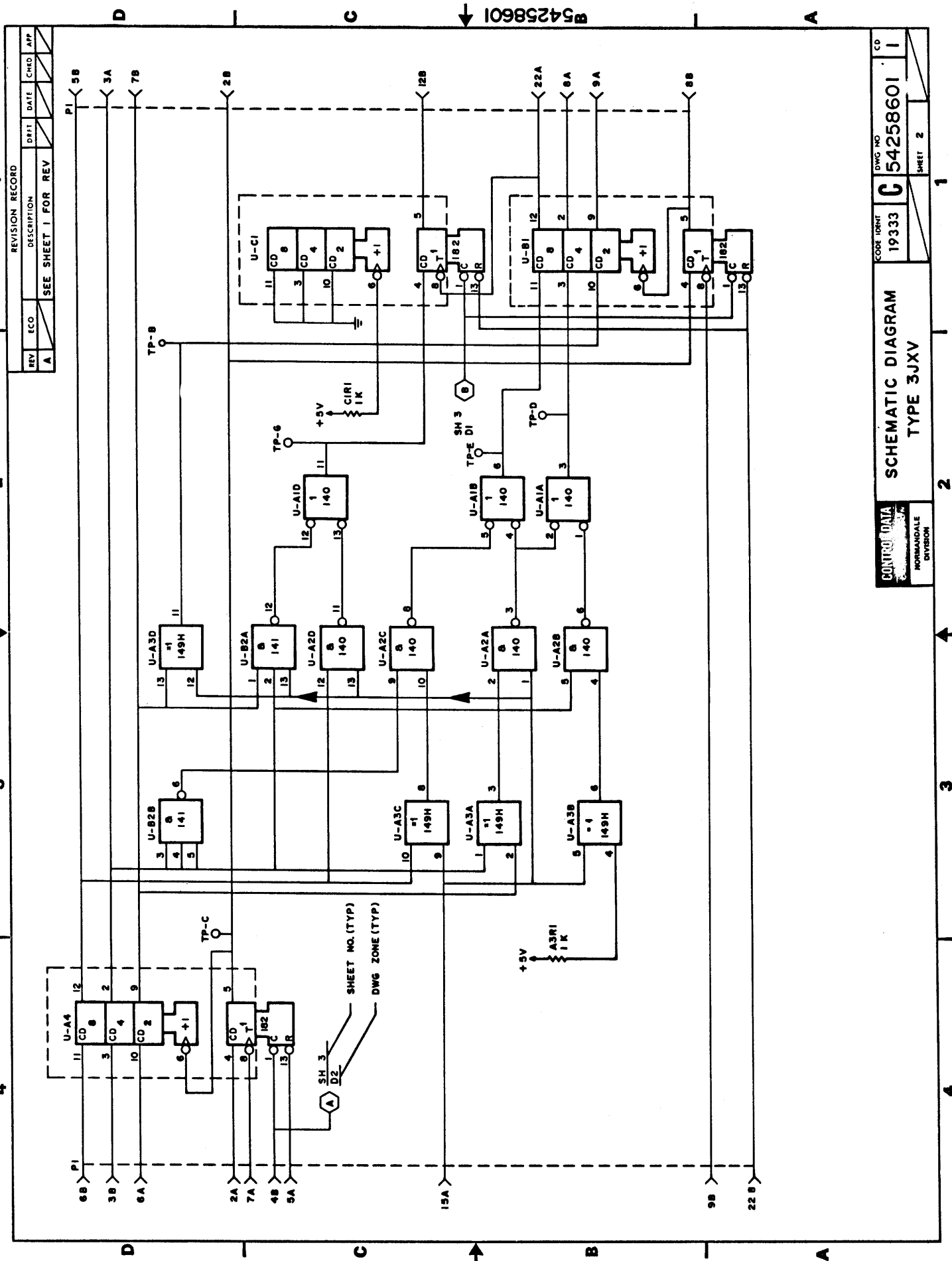
B54258201

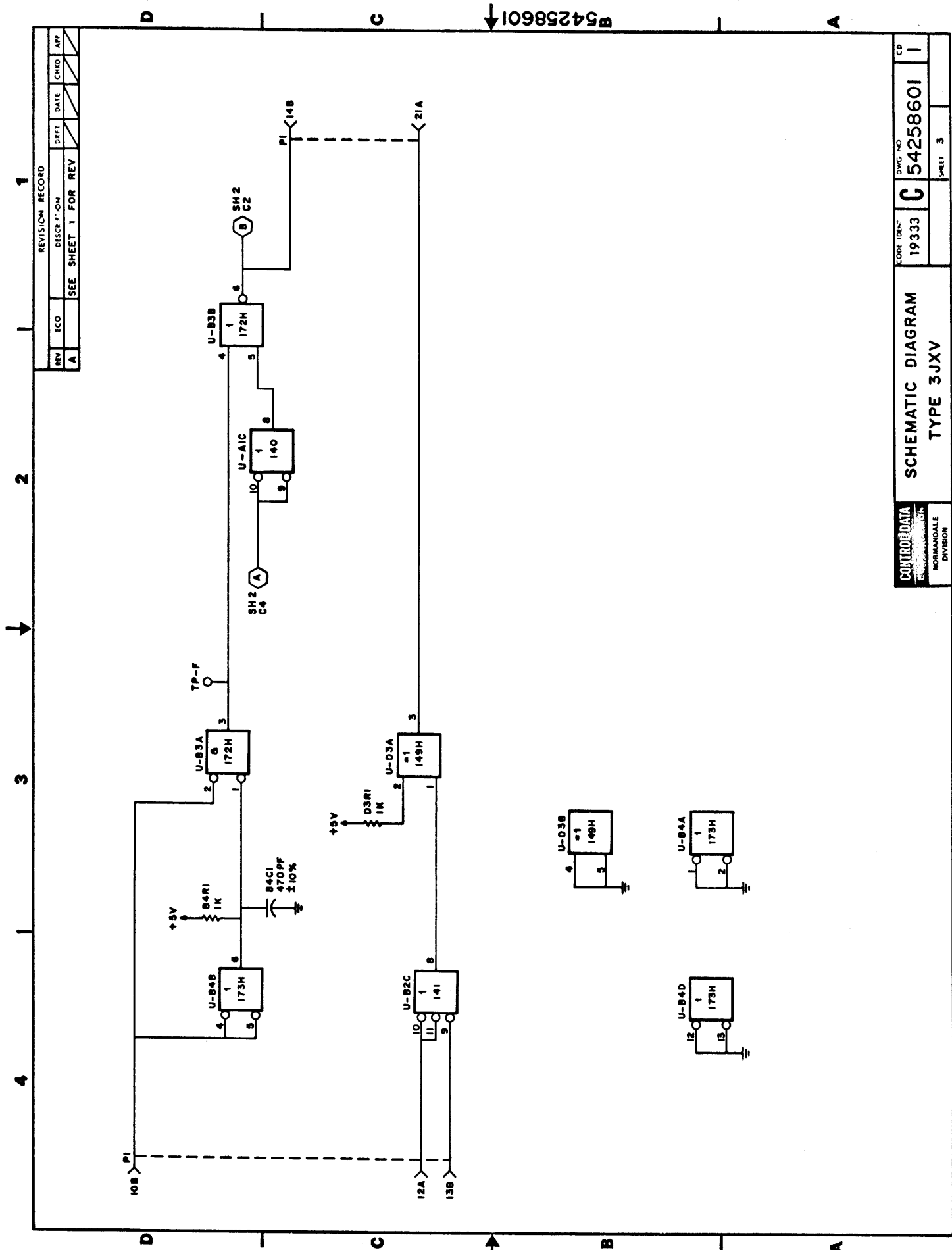


70616800 J









CONTROL DATA		SCHEMATIC DIAGRAM		CD	
NORMANDALE DIVISION		TYPE 3JXV		54258601	
		19333		C	
		DWG NO		54258601	
		SHEET		3	

1 2 3 4

1 2 3 4

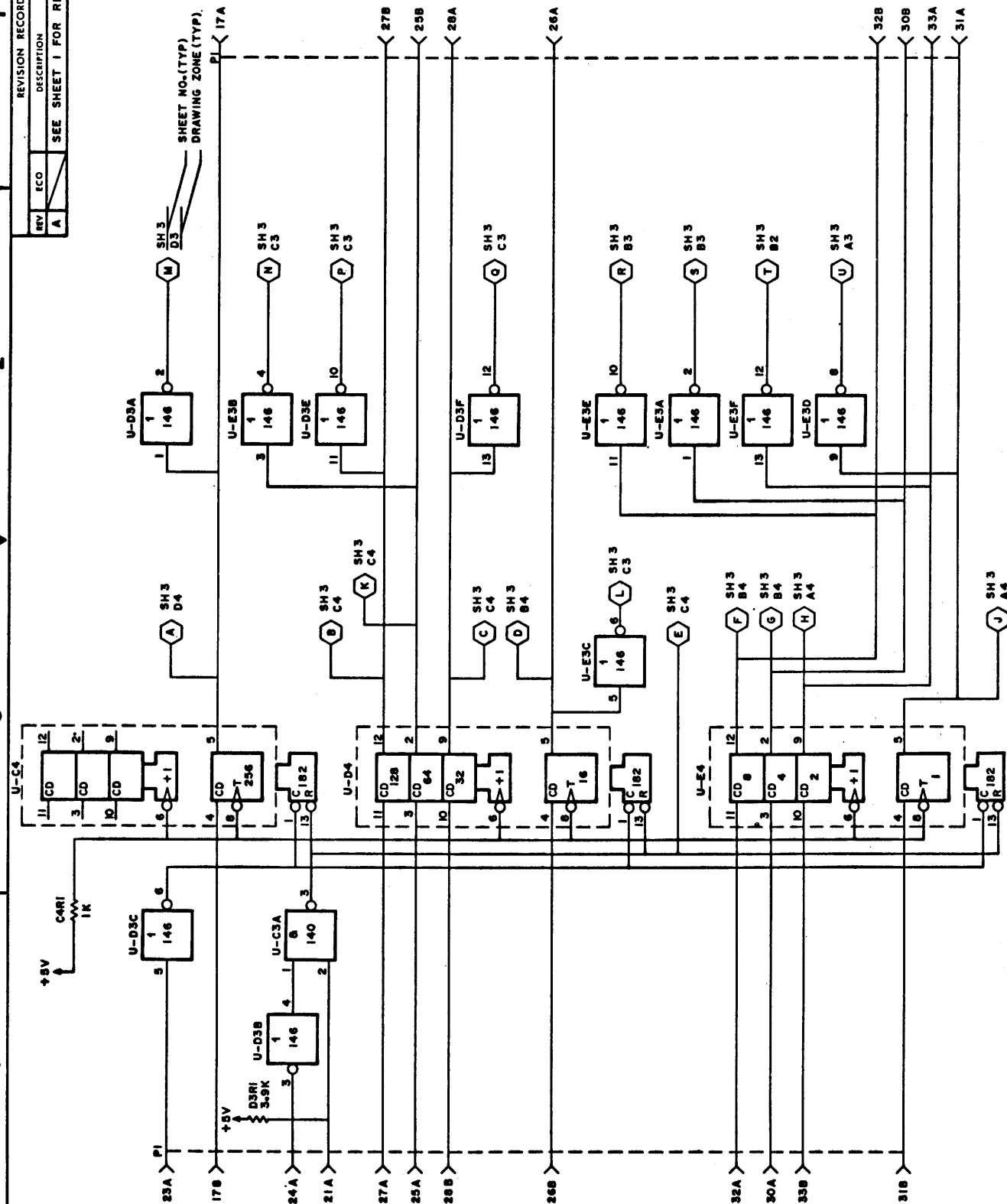
B54258601

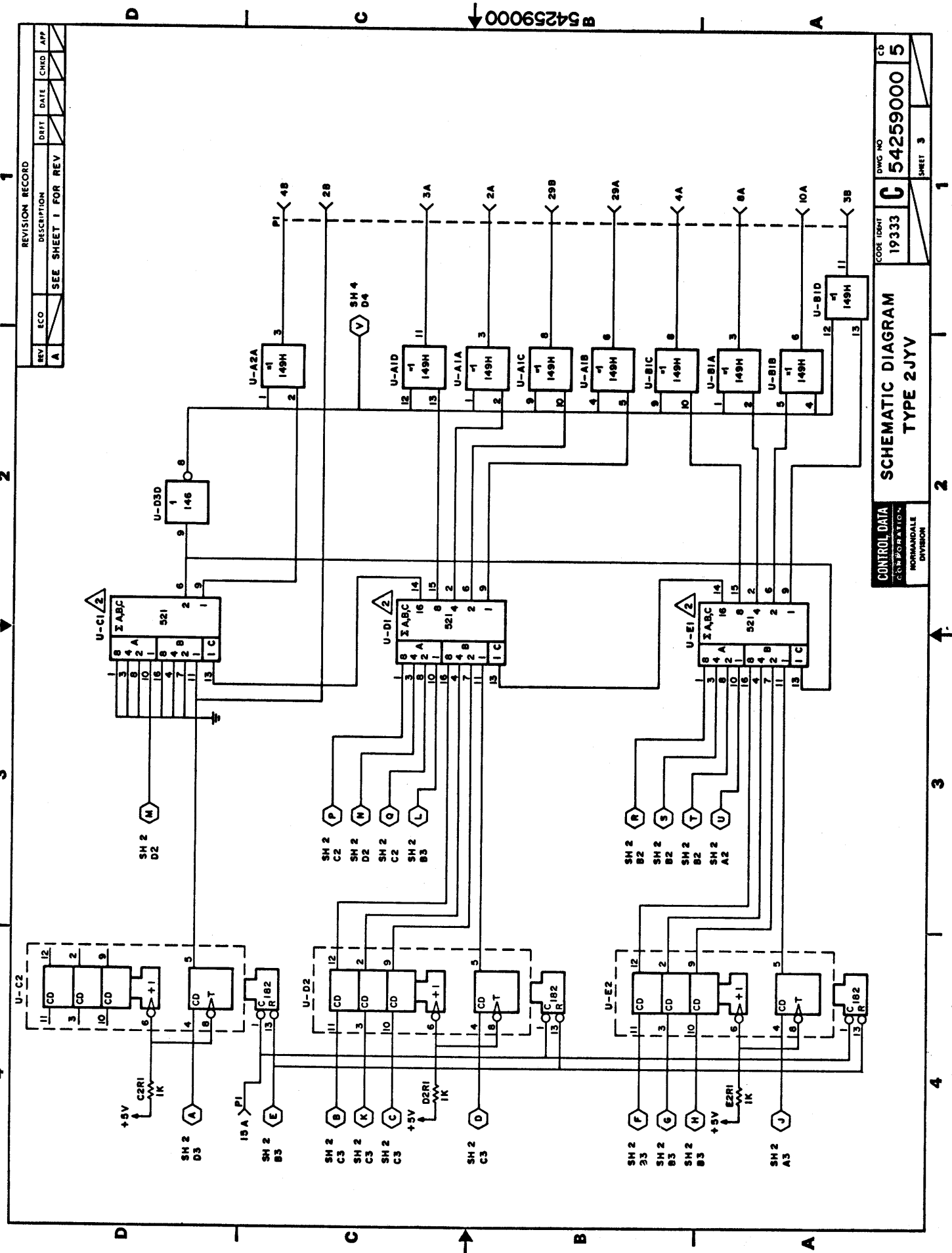
REVISION RECORD				
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A		SEE SHEET 1 FOR REV		

SHEET NO. (TYP)
DRAWING ZONE (TYP)

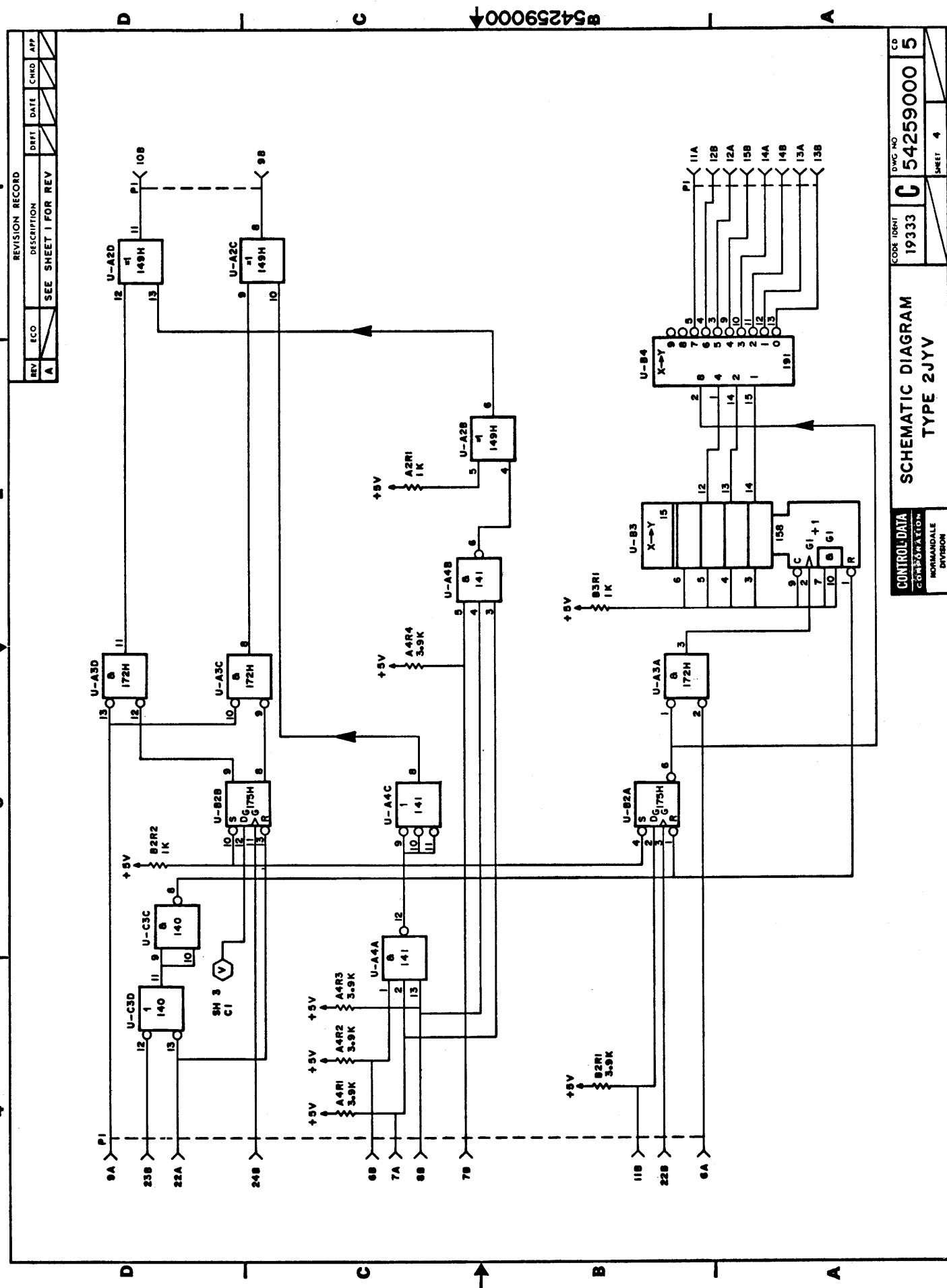
CONTROL DATA		DWG NO		SHEET	
CORPORATION		C		2	
NORMANDALE DIVISION		54259000		5	
		19333			

SCHEMATIC DIAGRAM TYPE 2JYV





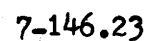
REVISION RECORD			
REV	ECO	DESCRIPTION	DATE
A		SEE SHEET 1 FOR REV	

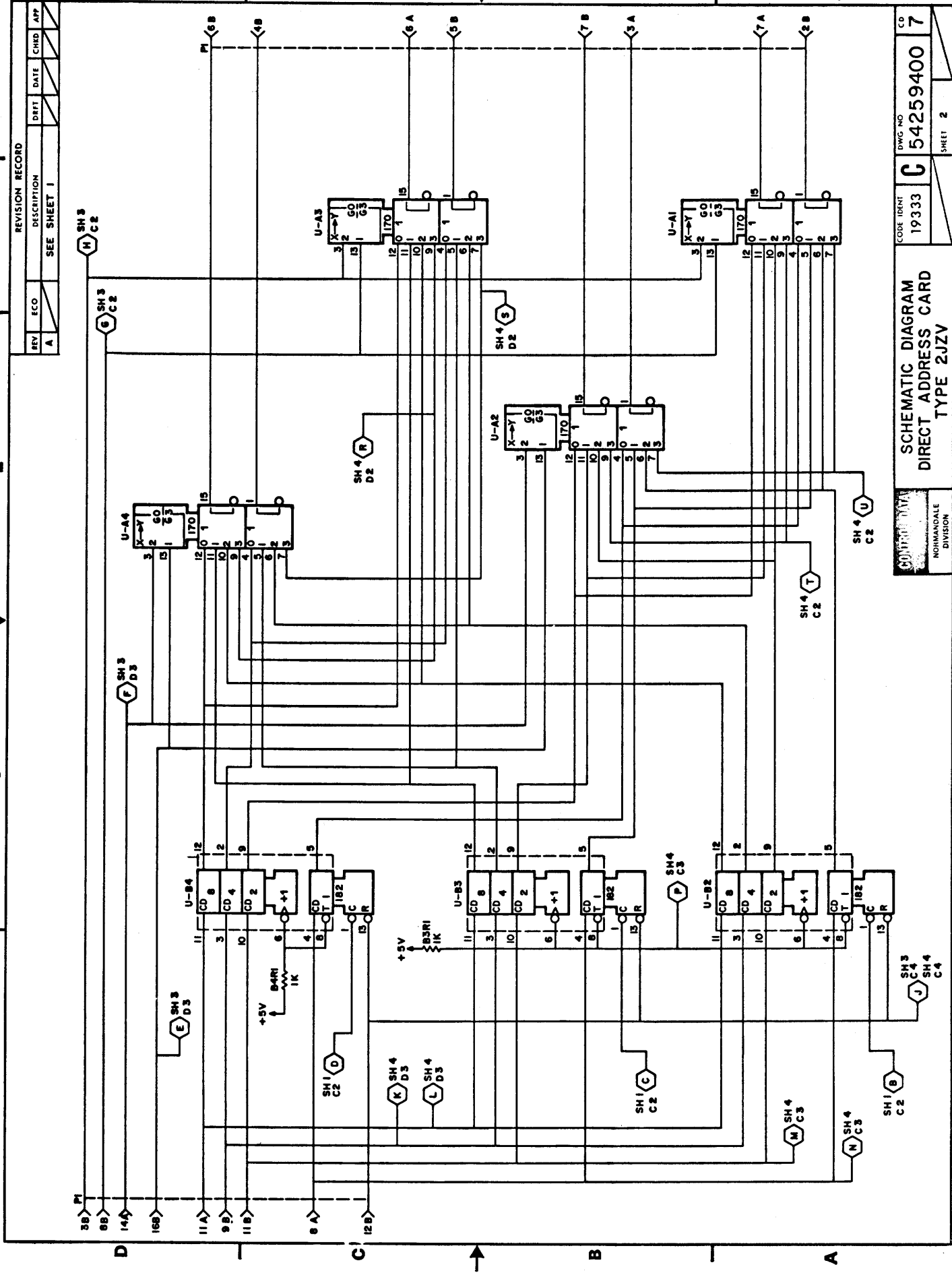


CONTROL DATA		DWG NO	
CORPORATION		C 54259000	
NORMANDALE DIVISION		SHEET 4	

SCHEMATIC DIAGRAM
TYPE 2JYV

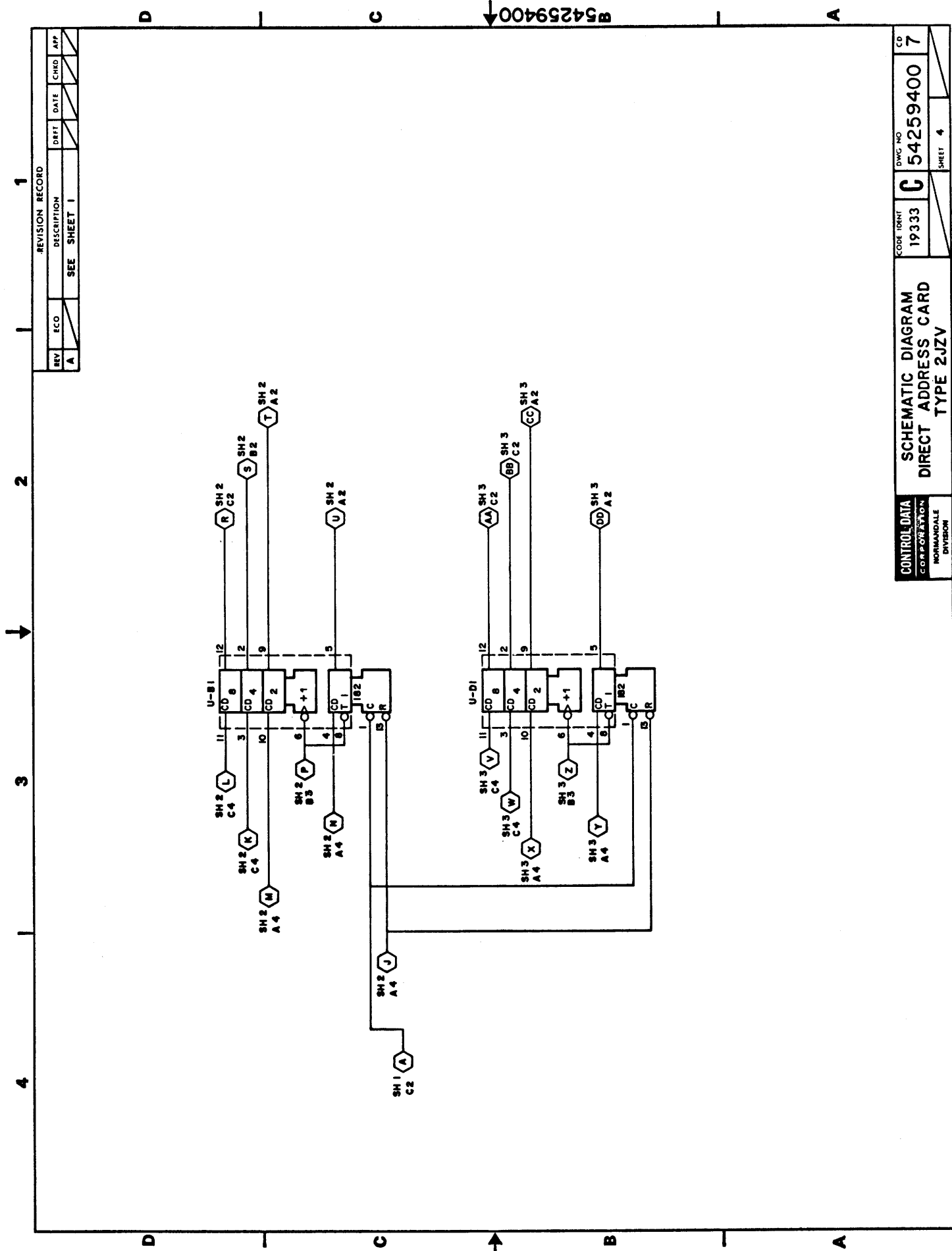
854259000





SCHEMATIC DIAGRAM DIRECT ADDRESS CARD TYPE 2JZV		CODE IDENT 19333	DWG NO C 54259400	SHEET 2
CONTINUED		NORMANDALE DIVISION		

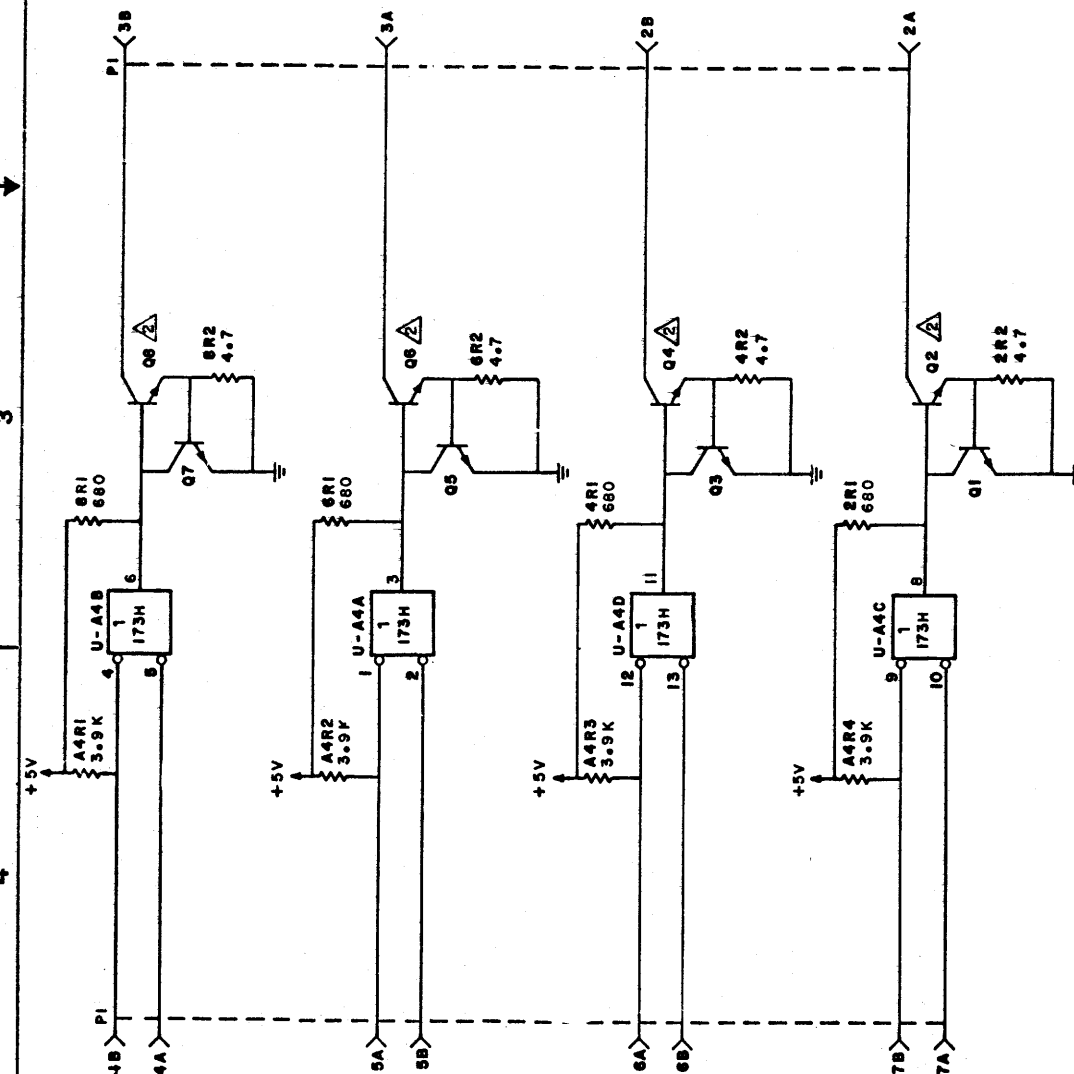
REVISION RECORD				
REV	ECO	DESCRIPTION	DATE	CHKD APP
A		SEE SHEET 1		



REV	ECO	DESCRIPTION	DATE	CHD	APP
A		SEE SHEET 1			

CONTROL DATA CORPORATION NORMANDALE DIVISION		SCHEMATIC DIAGRAM DIRECT ADDRESS CARD TYPE 2JZV		CODE DENT 19333	DWG NO 54259400	CD 7
				SHEET 4		

B54259400

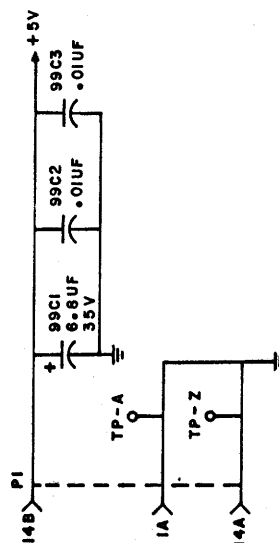


NOTE:

1 UNLESS OTHERWISE SPECIFIED

ALL TRANSISTORS, SILICON NPN 2N3646
50210310

2 TRANSISTORS SILICON NPN 2N3569 50210811

3 ALL INTEGRATED CIRCUITS HAVE PIN 7
CONNECTED TO GND AND PIN 14 CONNECTED
TO +5V

SHEET REVISION STATUS		REVISION RECORD			
REV	ECO	DESCRIPTION	DATE	CHKD	APP
A		RELEASED	6-3-70		
B		DOC SIZE & SYM CHANGE	6-3-70		
C		PE29310			
D		PE23000			

REFERENCE DRAWINGS		CONTROLDATA		NORMANDALE DIVISION	
COMP ASSY	54120100	FIRST	5-19-70	VCD	
COMPONENTS EXCEPT AS NOTED		CHK	6-3-70	ENGR	7-10-70
TOLERANCE	VALUE	WFC	6-12-70	APPR	6-12-70
RES	± 5 %				
CAP	± 20 %				
SCHEMATIC DIAGRAM LAMP DRIVER TYPE 0 PAV		CODE IDENT	19333	DRAWING NUMBER	54120200
					8
					CD
					1 OF 2

A

C

B 54120200

D

1

2

3

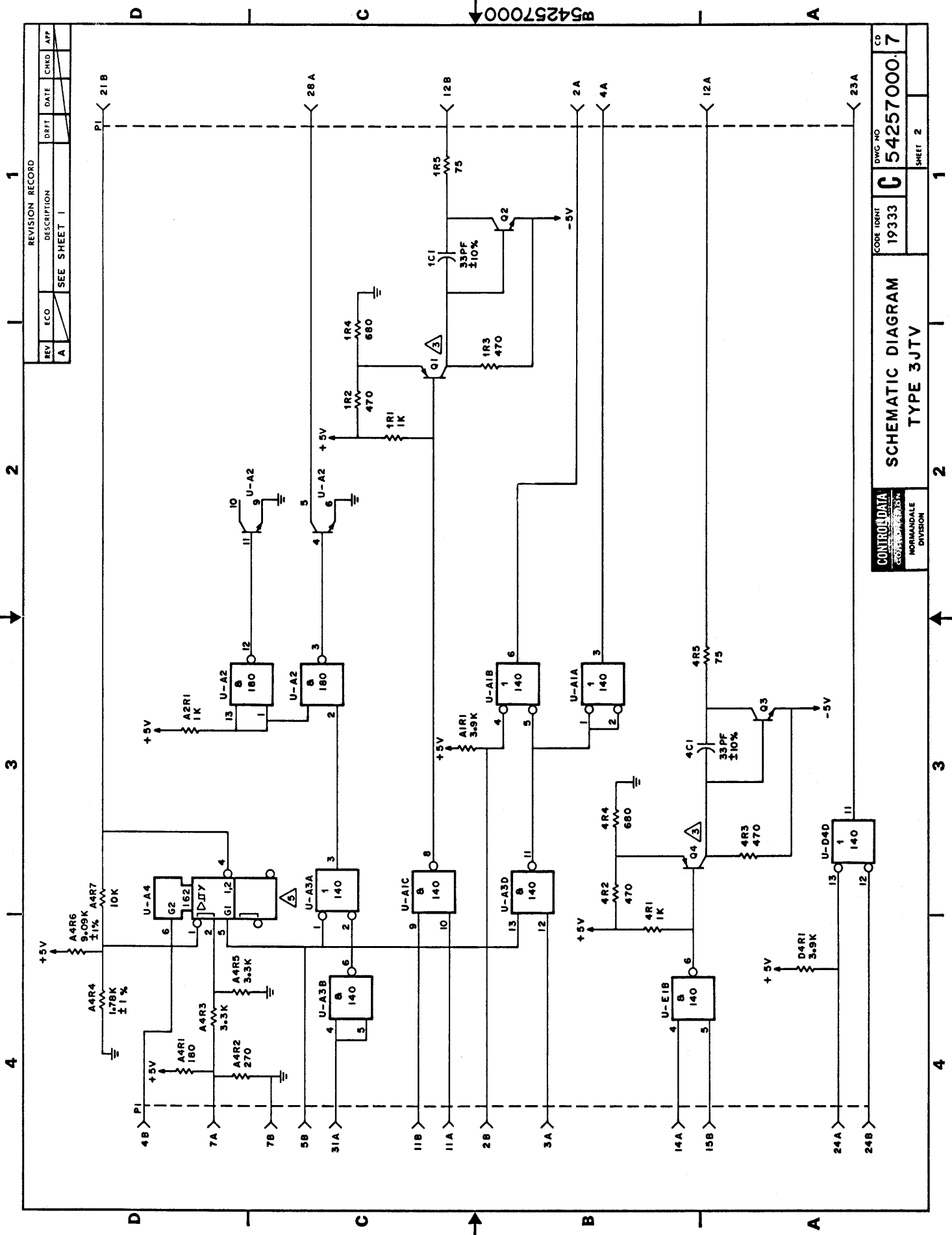
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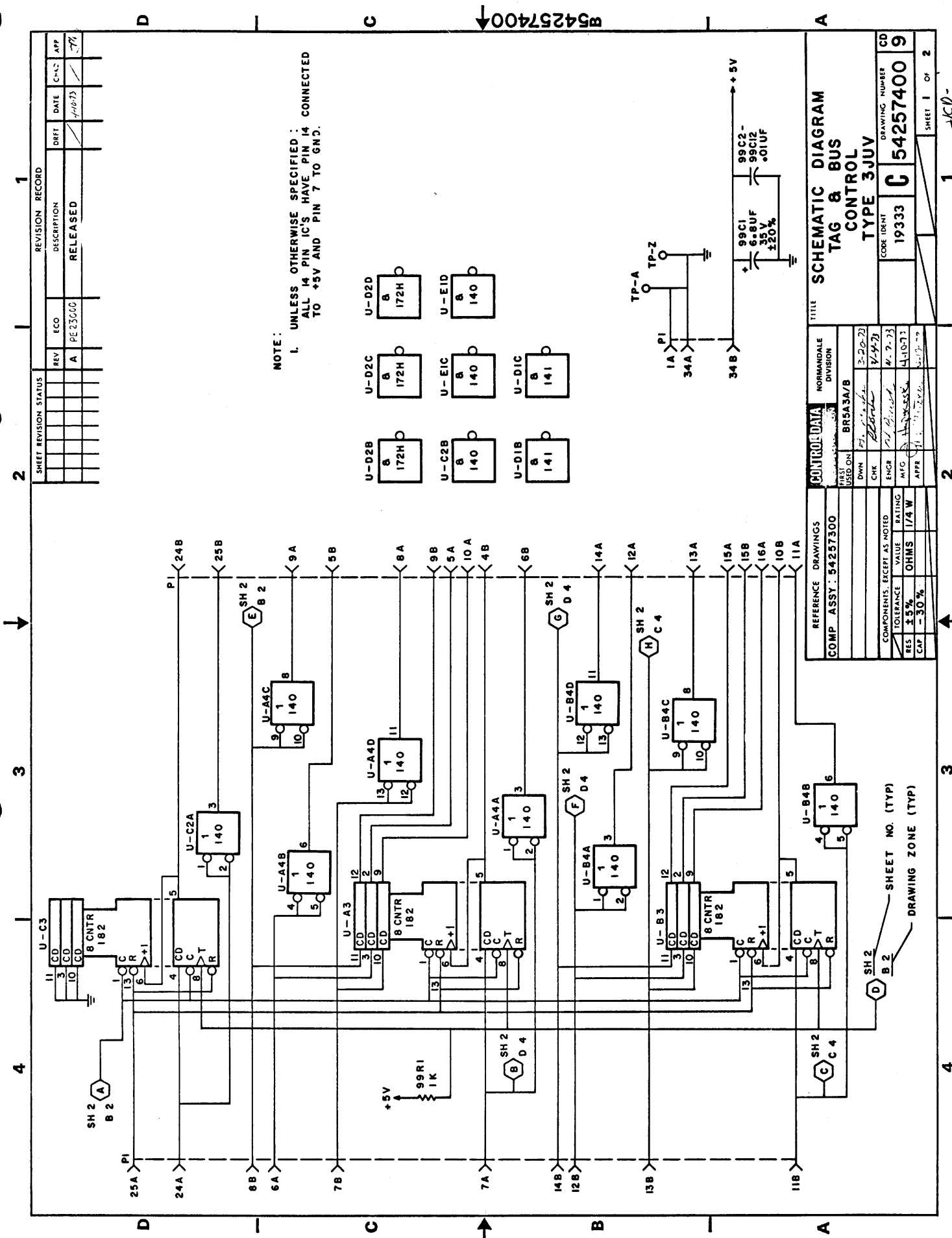
1

2

3

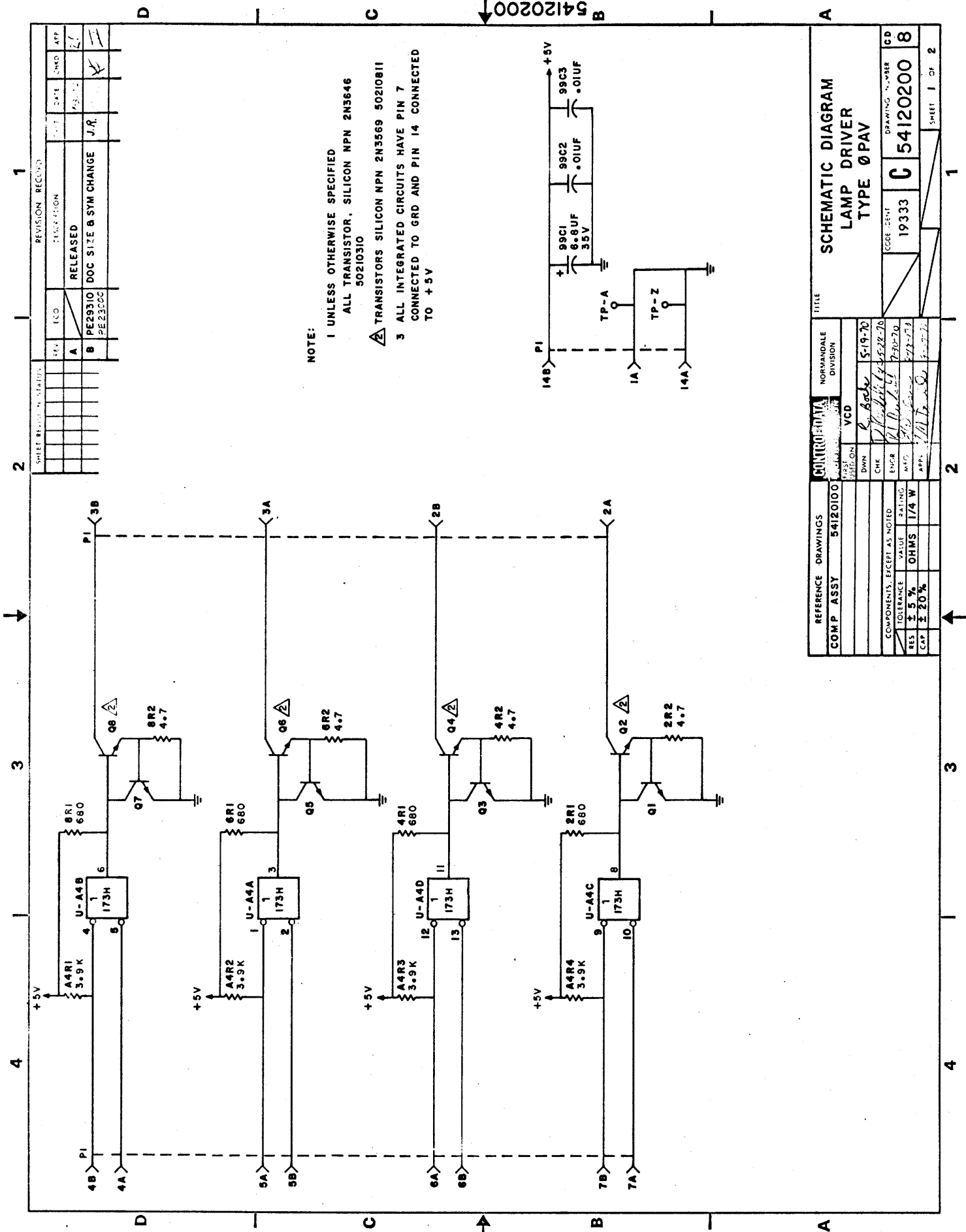
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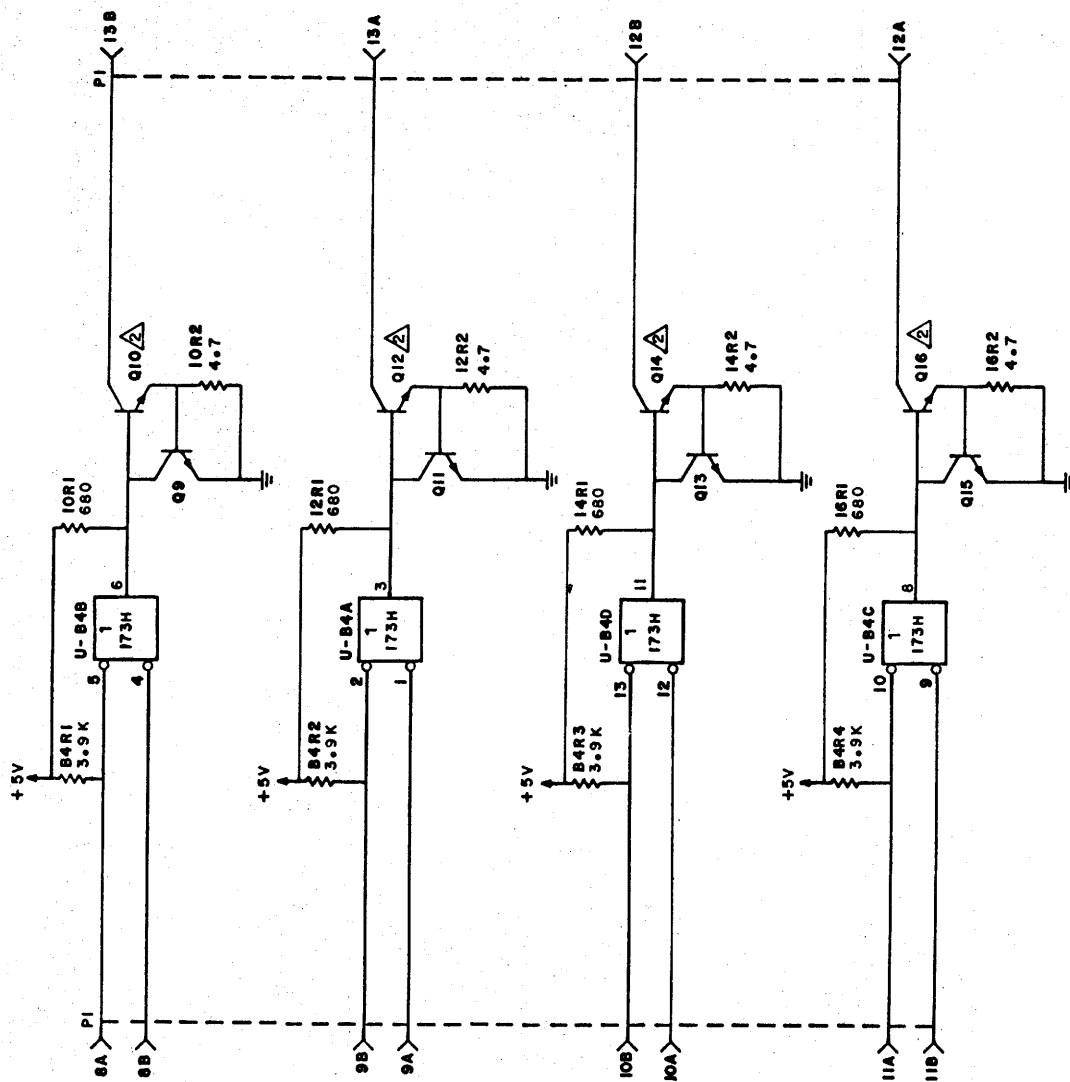
B54257400







CONTROL DATA CORPORATION		NORMANDALE DIVISION	
SCHEMATIC DIAGRAM LAMP DRIVER TYPE ØPAV			
CODE IDENT	19333	DWG NO	C 54120200
		SHEET 2	
		8	



REVISION RECORD

DESCRIPTION

SEE SHT 1 FOR REVISION

REV

ECO

B

DATE

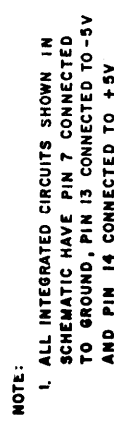
CHKD

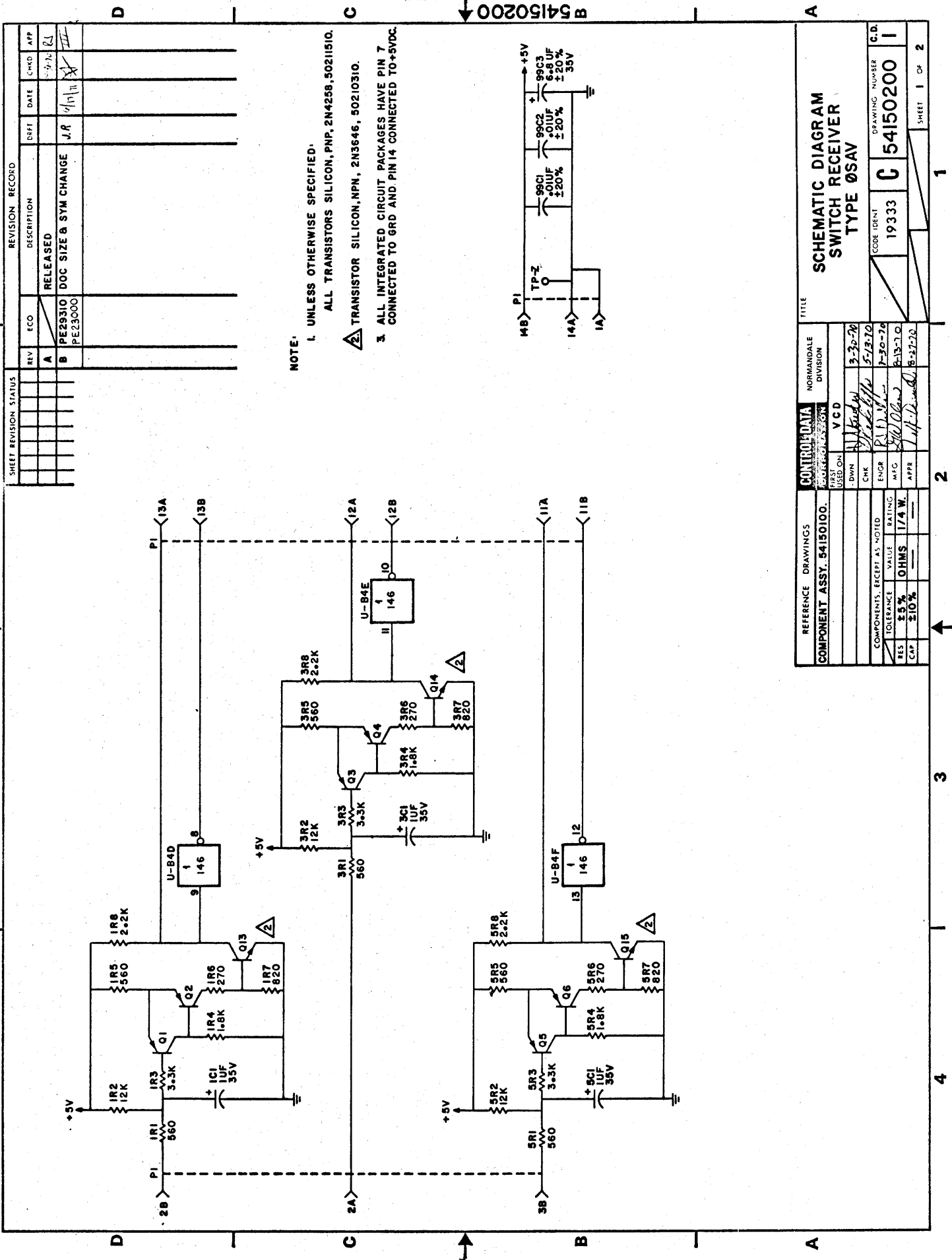
APP

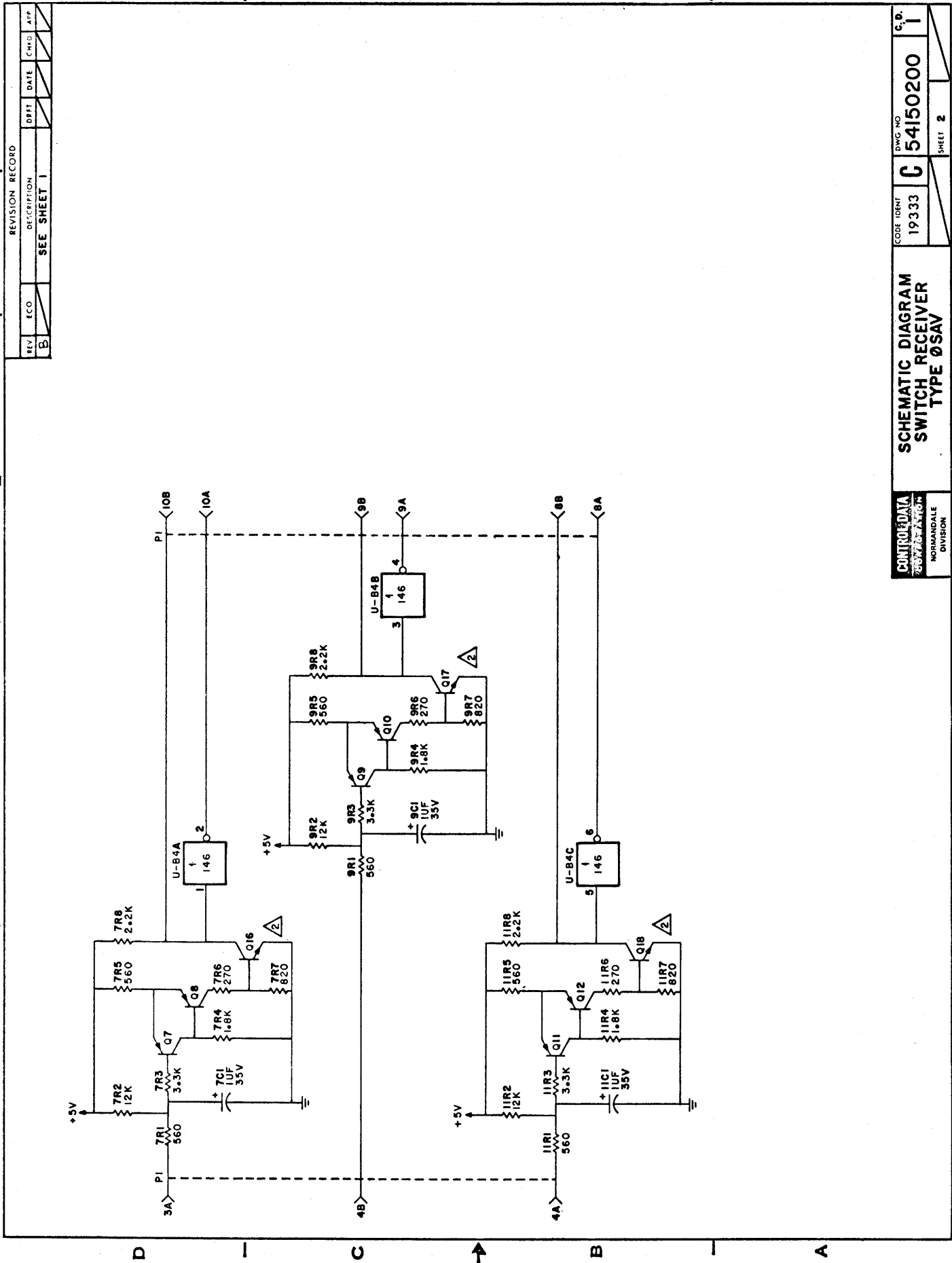
B 54120200







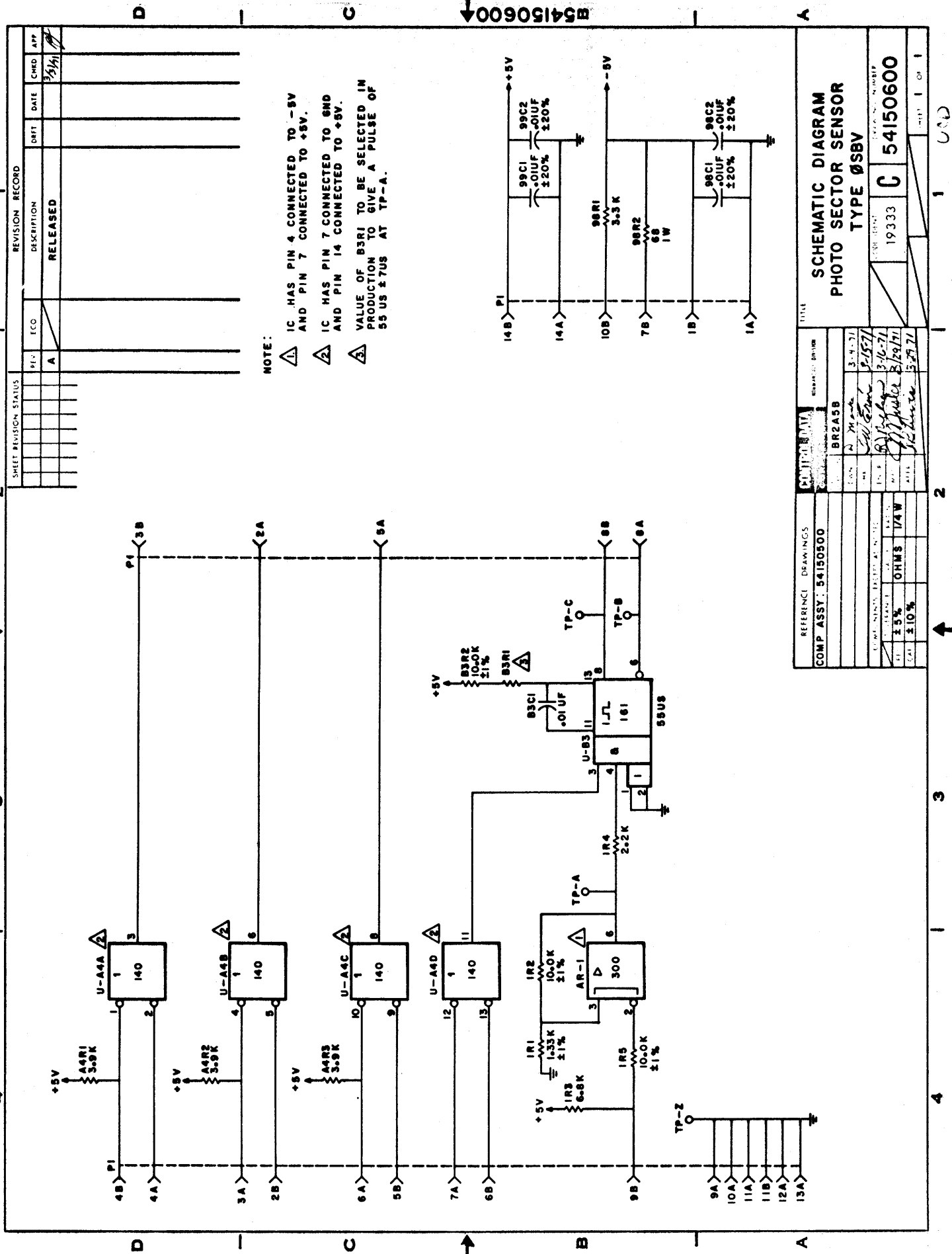




REVISION RECORD			
REV	ECO	DESCRIPTION	DATE
B		SEE SHEET 1	
1			

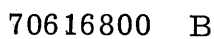
CONTROL DATA CORPORATION	SCHEMATIC DIAGRAM	DWG NO	54150200
	SWITCH RECEIVER	CODE IDENT	19333
	TYPE ØSAV	SHEET	2
1			

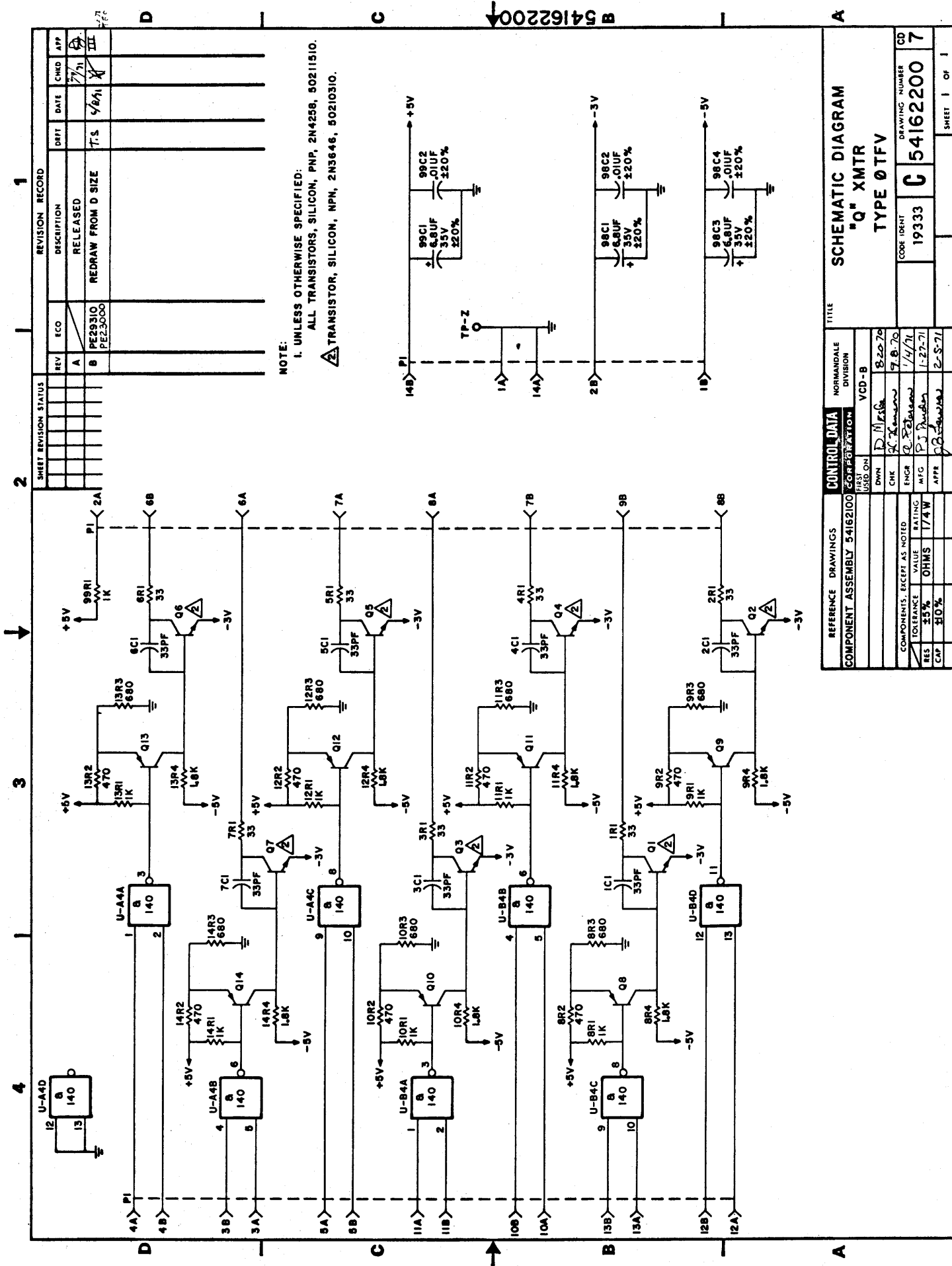
B 54150200



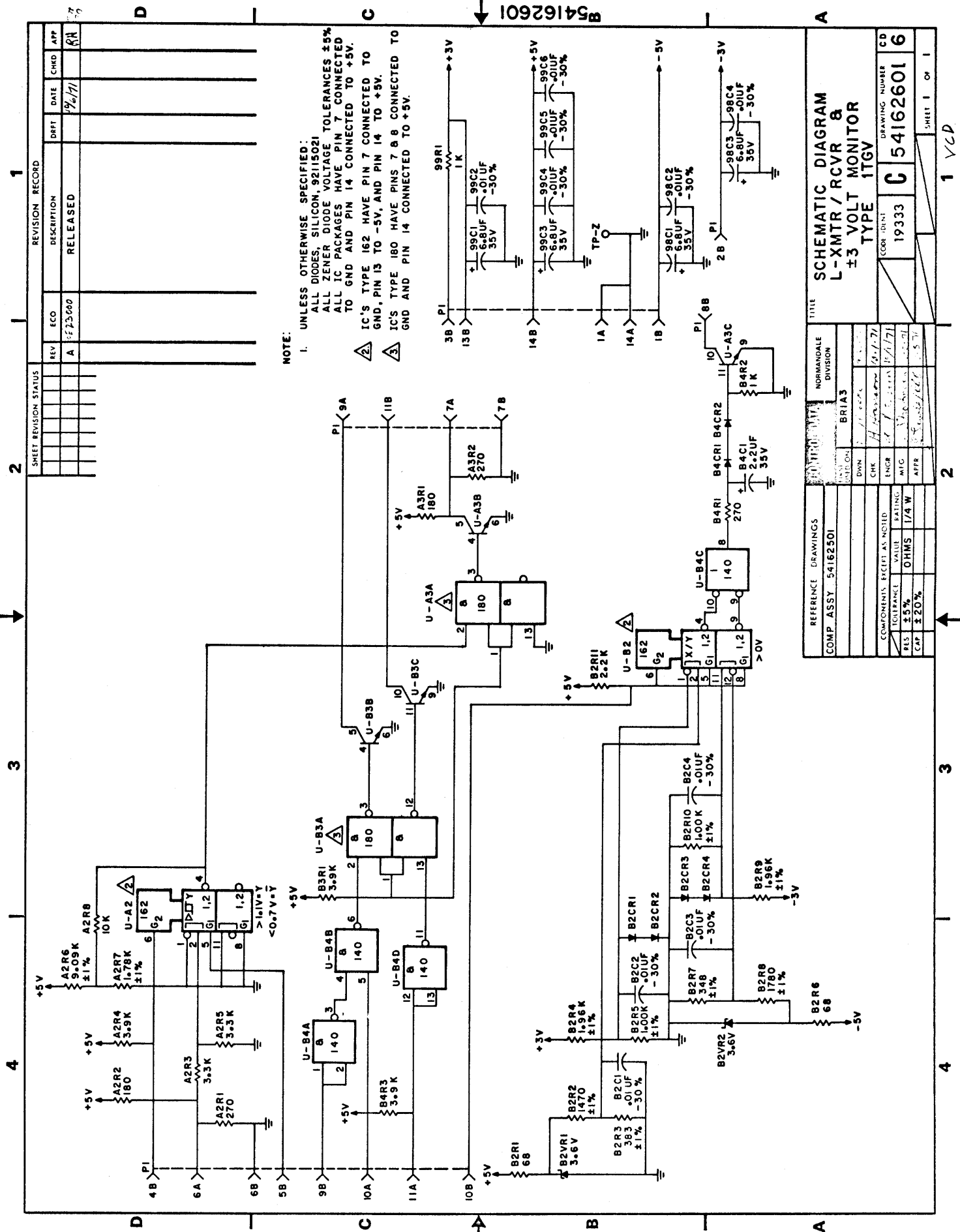
B54150600



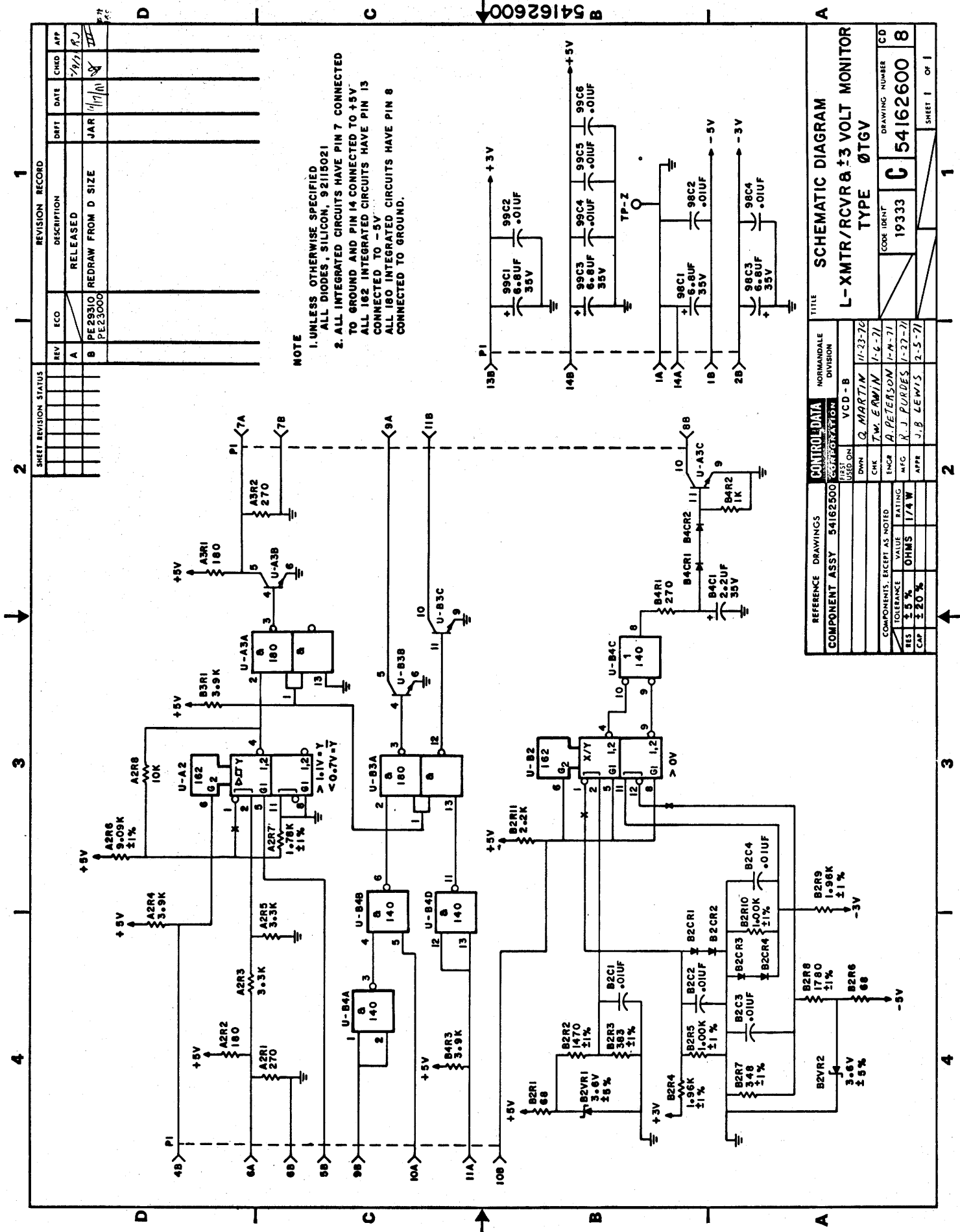


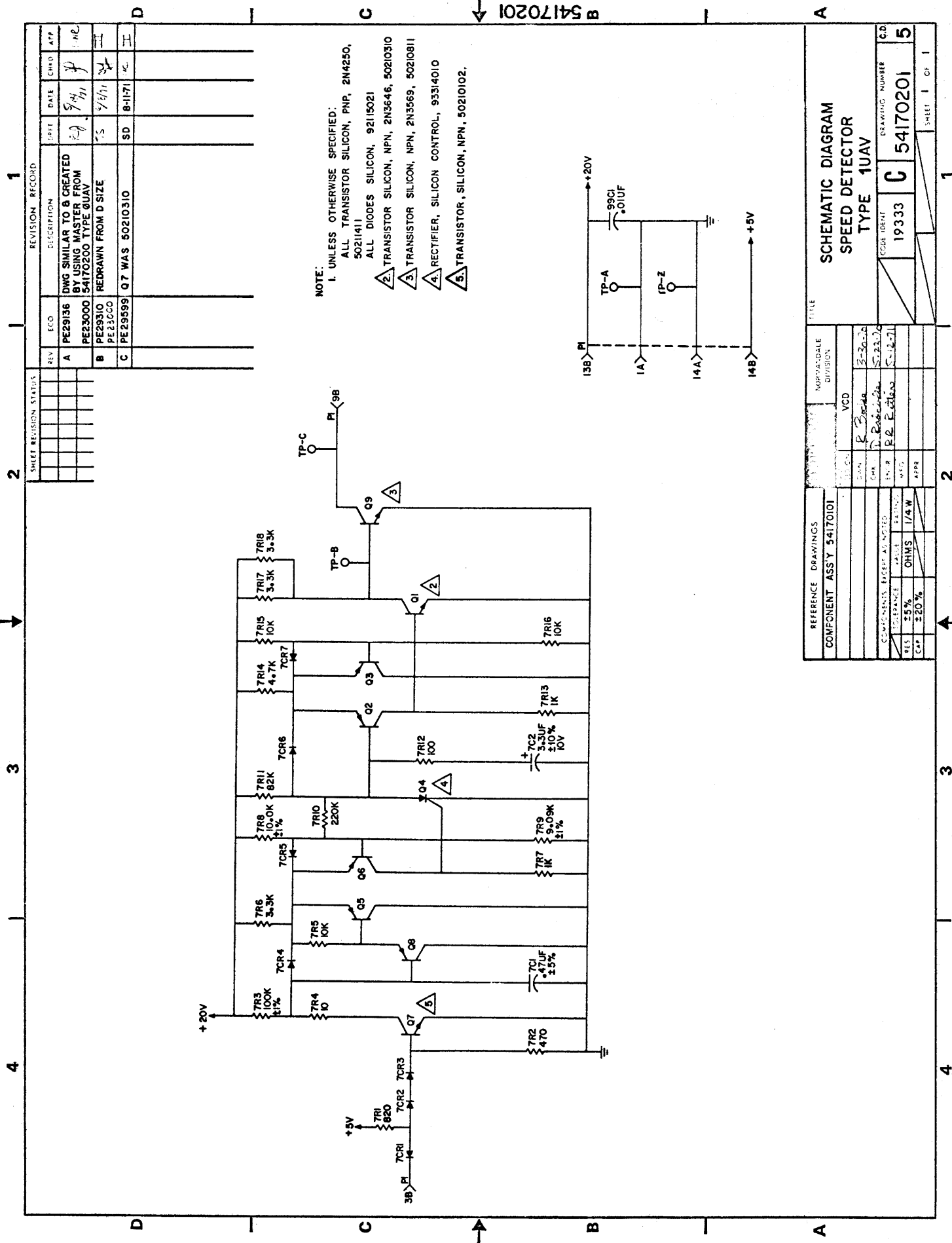


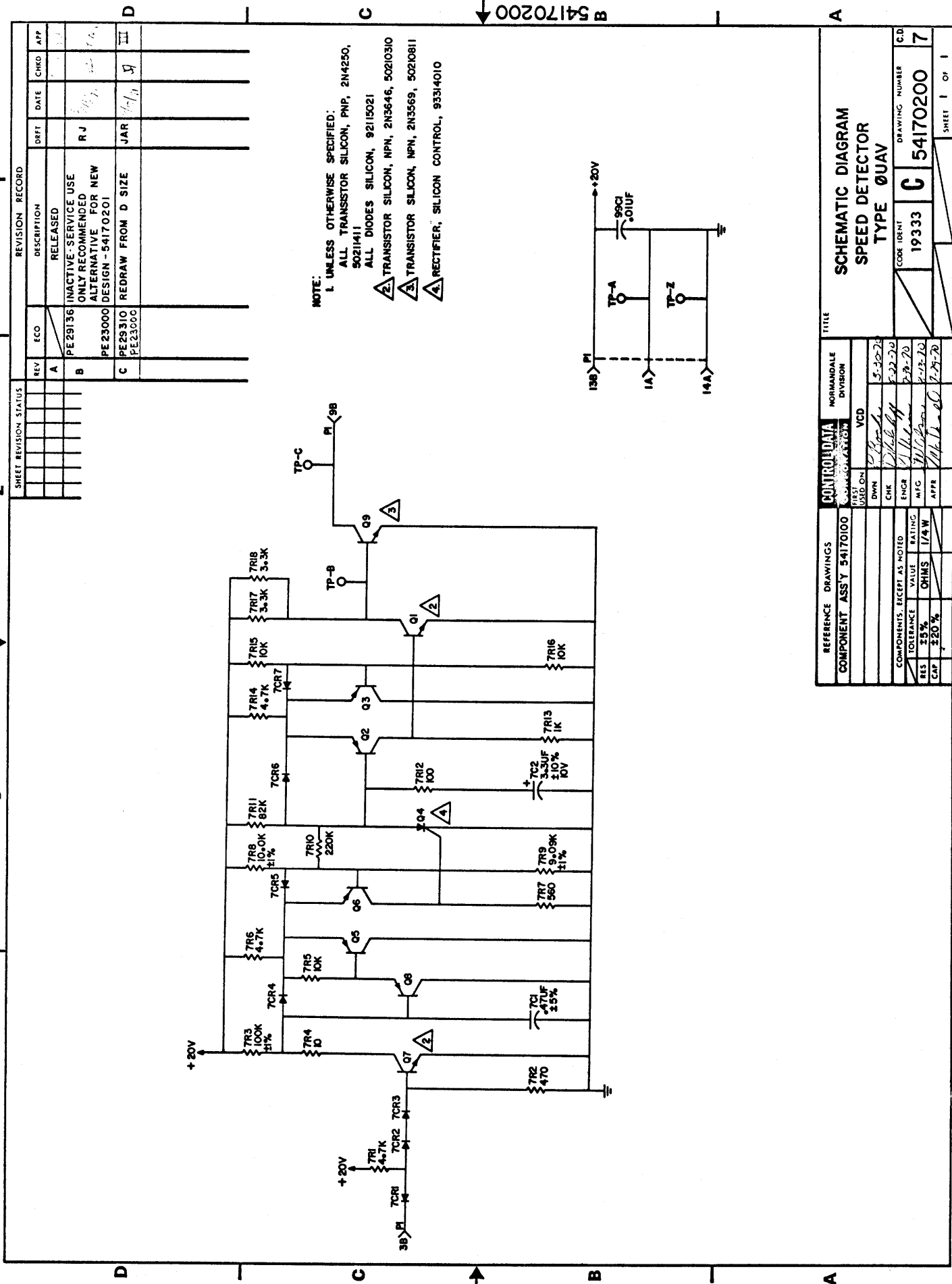
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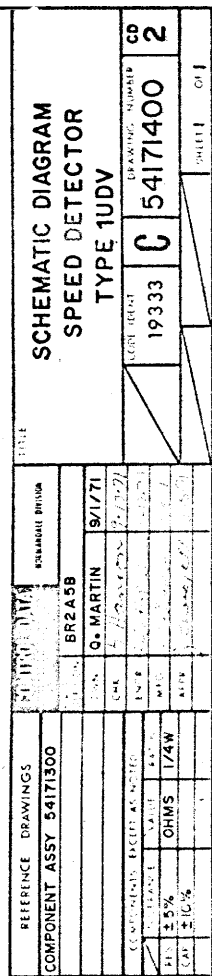






SHEET REVISION STATUS				REVISION RECORD			
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A	PE29136	RELEASED					
B	PE23000	INACTIVE-SERVICE USE ONLY RECOMMENDED ALTERNATIVE FOR NEW DESIGN - 54170201	RJ				
C	PE29310	REDRAW FROM D SIZE	JAR				
D	PE23000						

REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMPONENT ASSY 54170100		54170200		VCD		SCHEMATIC DIAGRAM	
						SPEED DETECTOR	
						TYPE 0UAV	
						DRAWING NUMBER	
						19333	
						C 54170200	
						7	
						SHEET 1 OF 1	

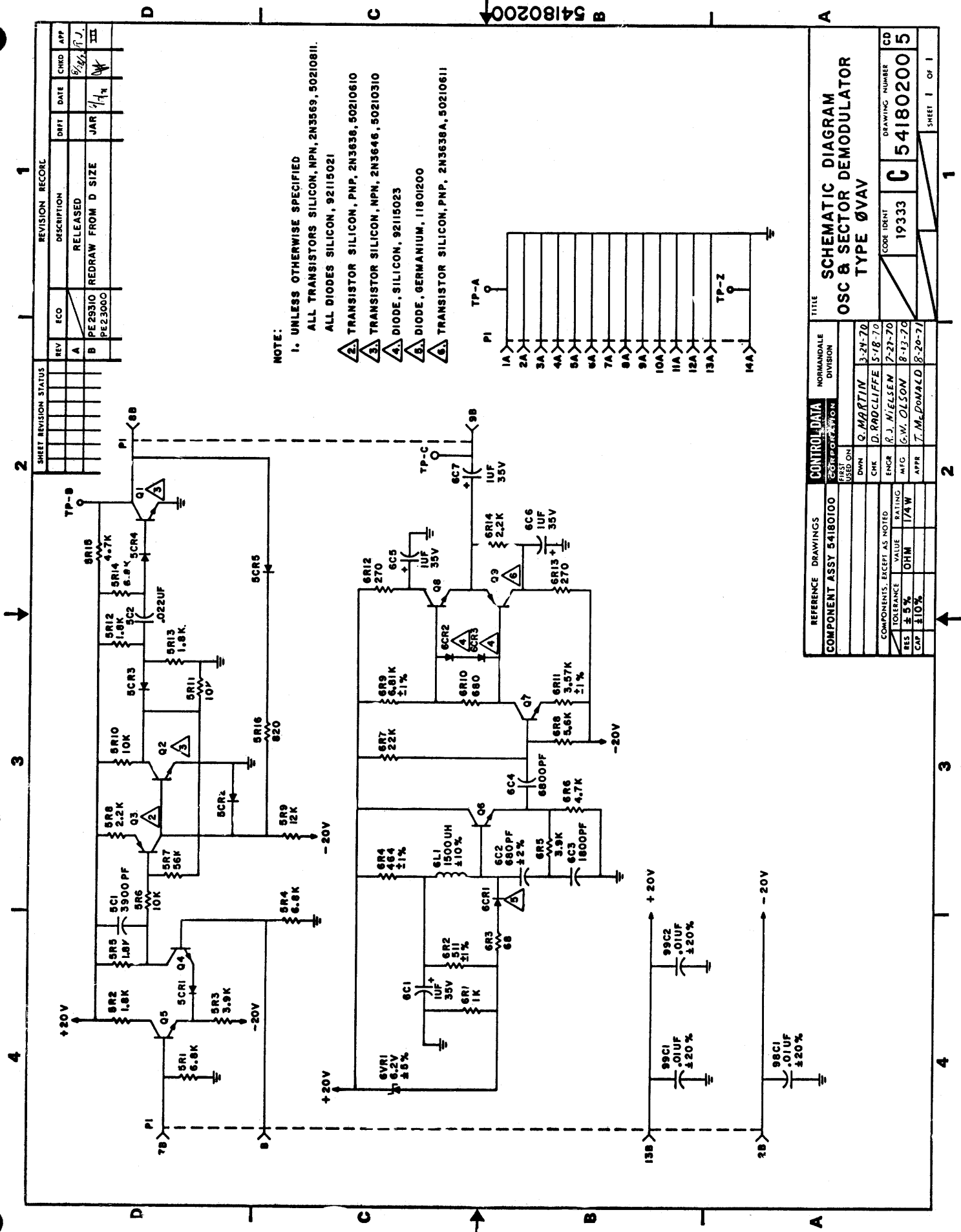


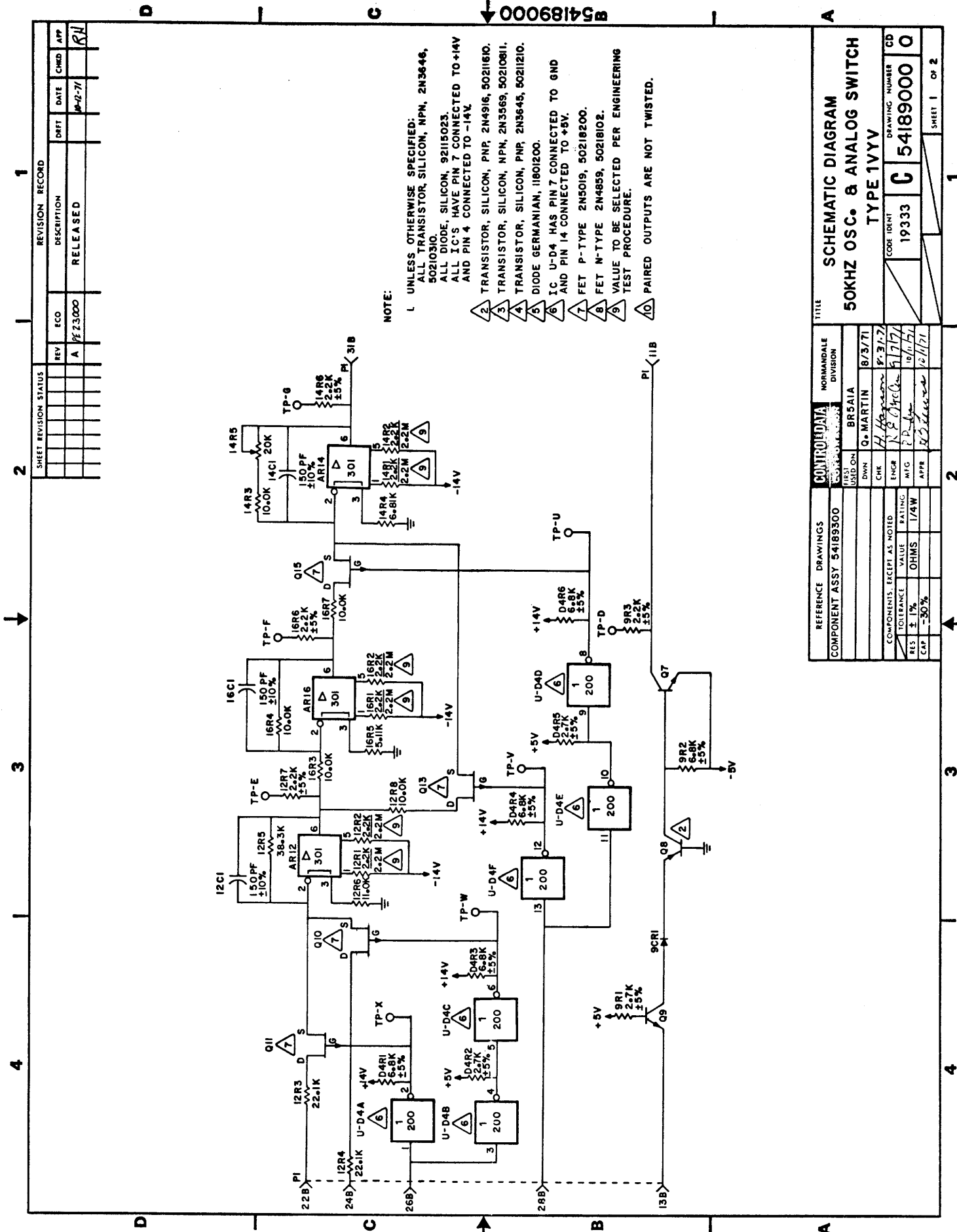
SCHEMATIC DIAGRAM
SPEED DETECTOR
TYPE 1UDV

19333	C	54171400	DRAWING, STANDARD
-------	---	----------	-------------------

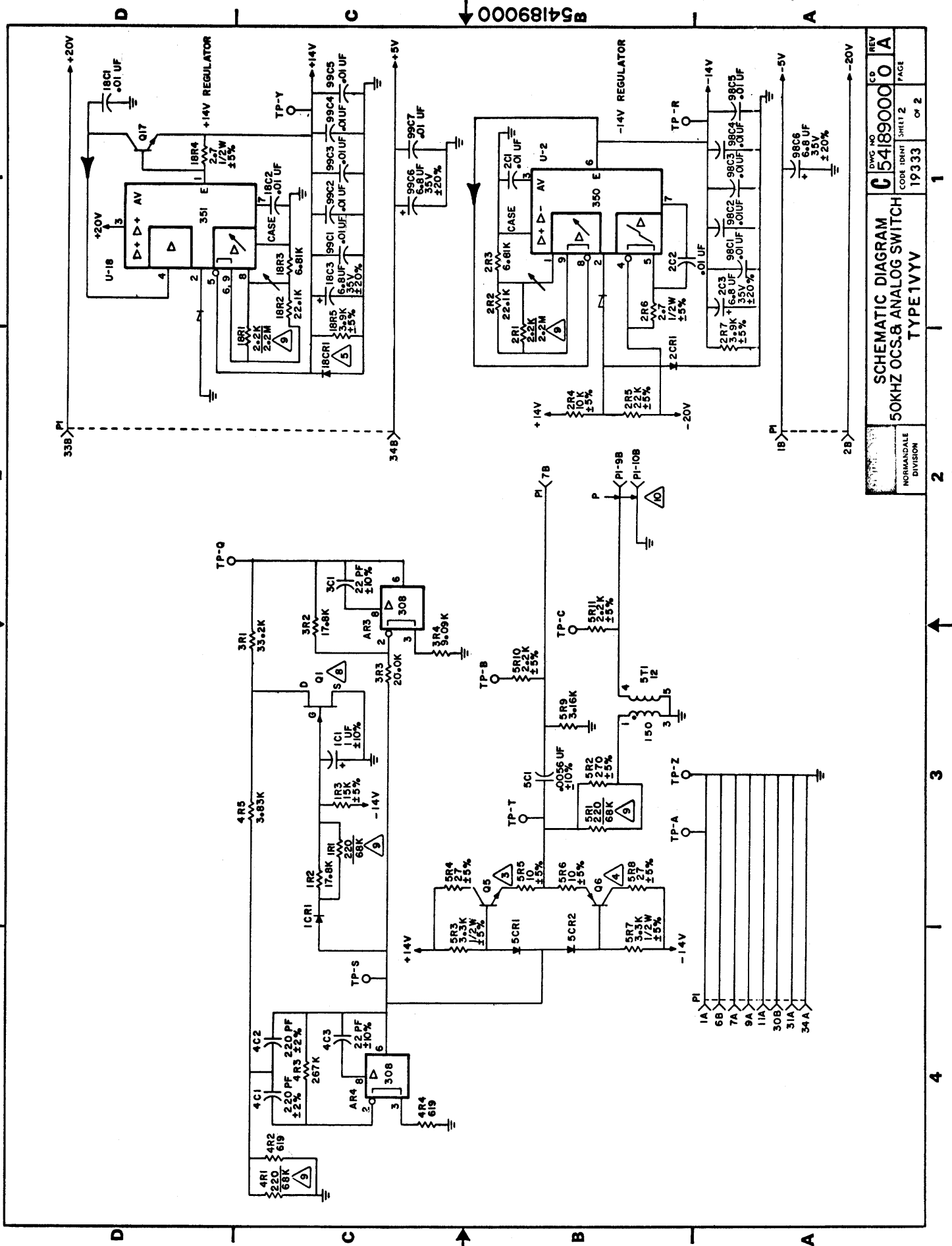
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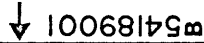
VC D

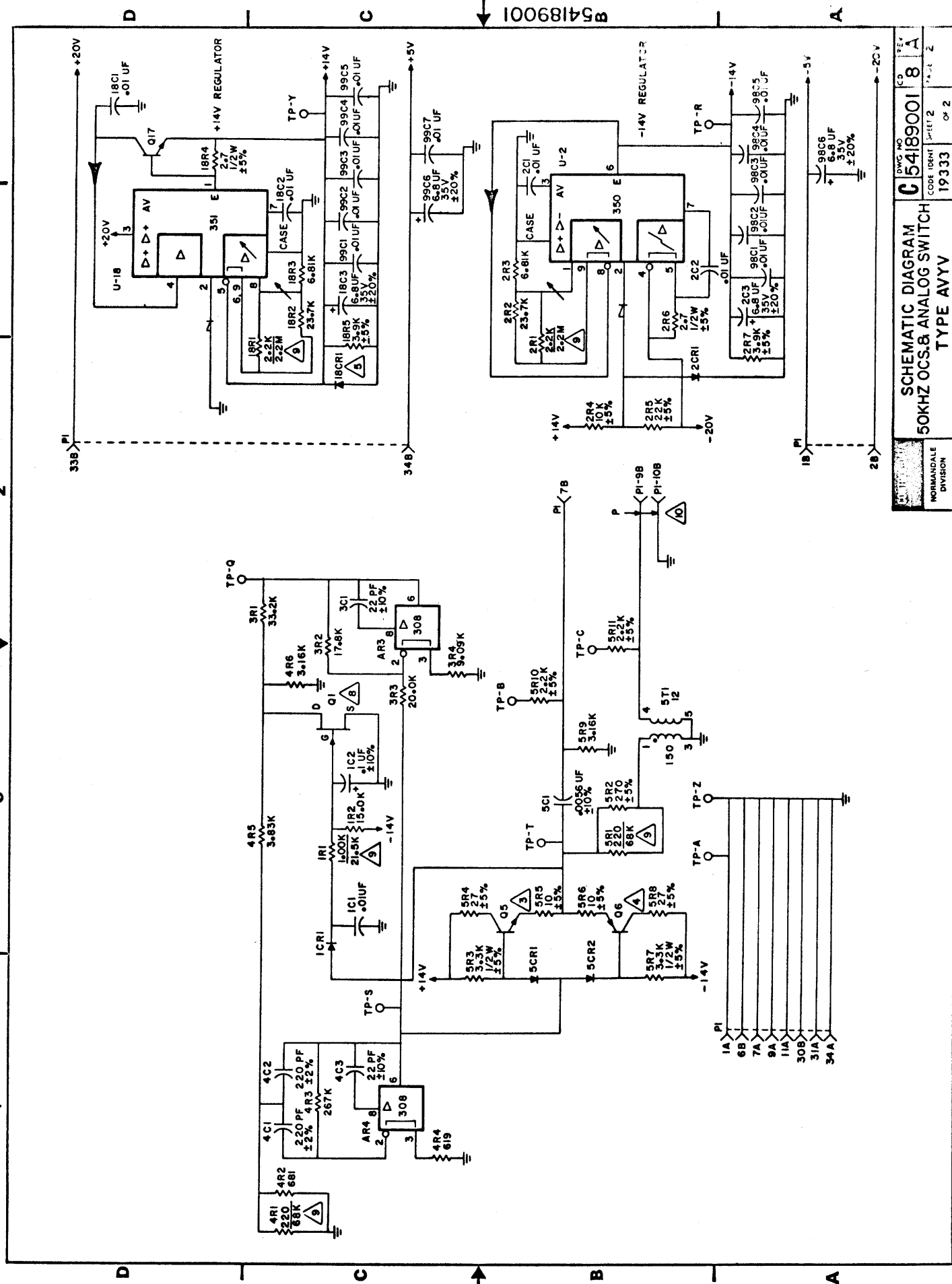


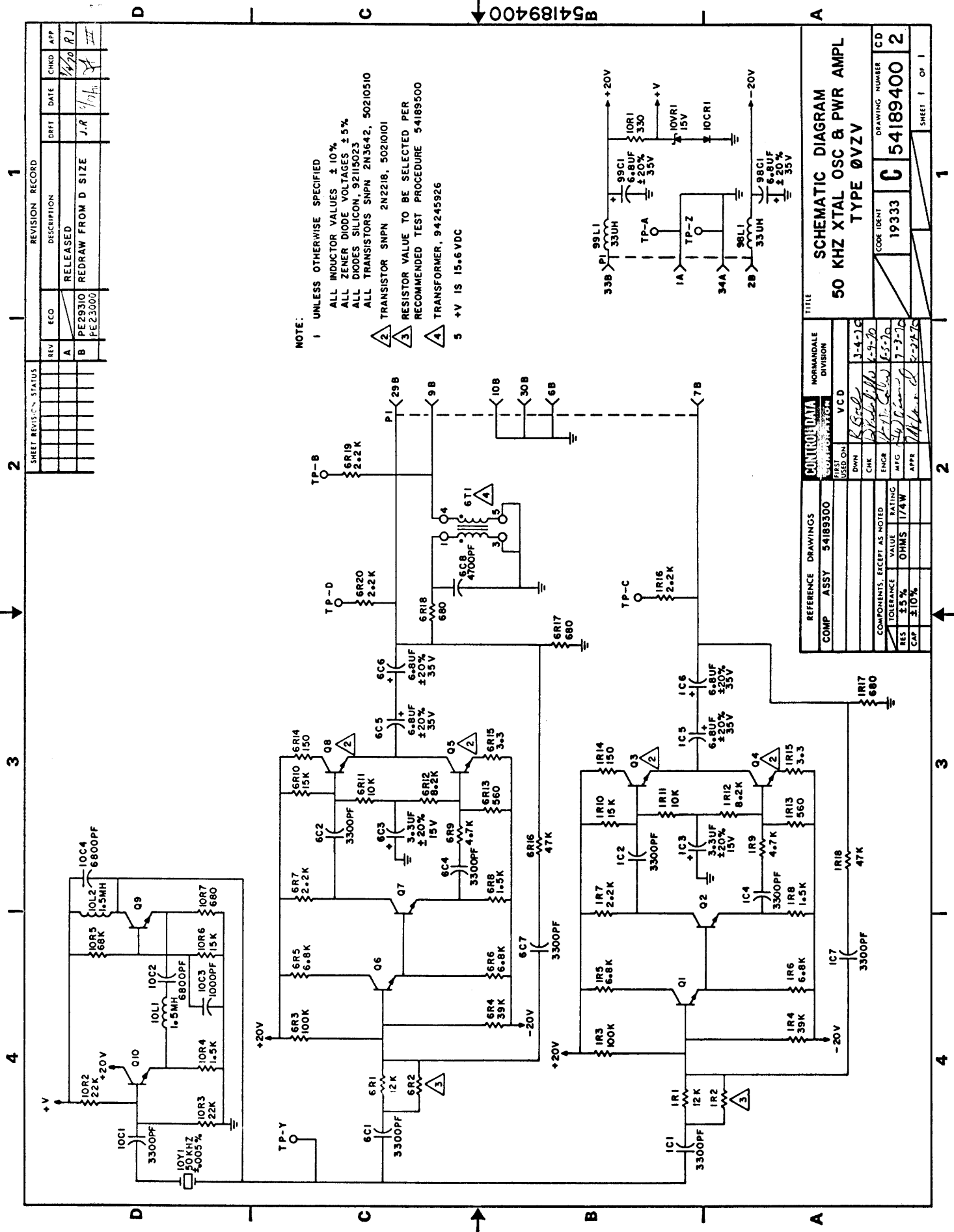


B54189000



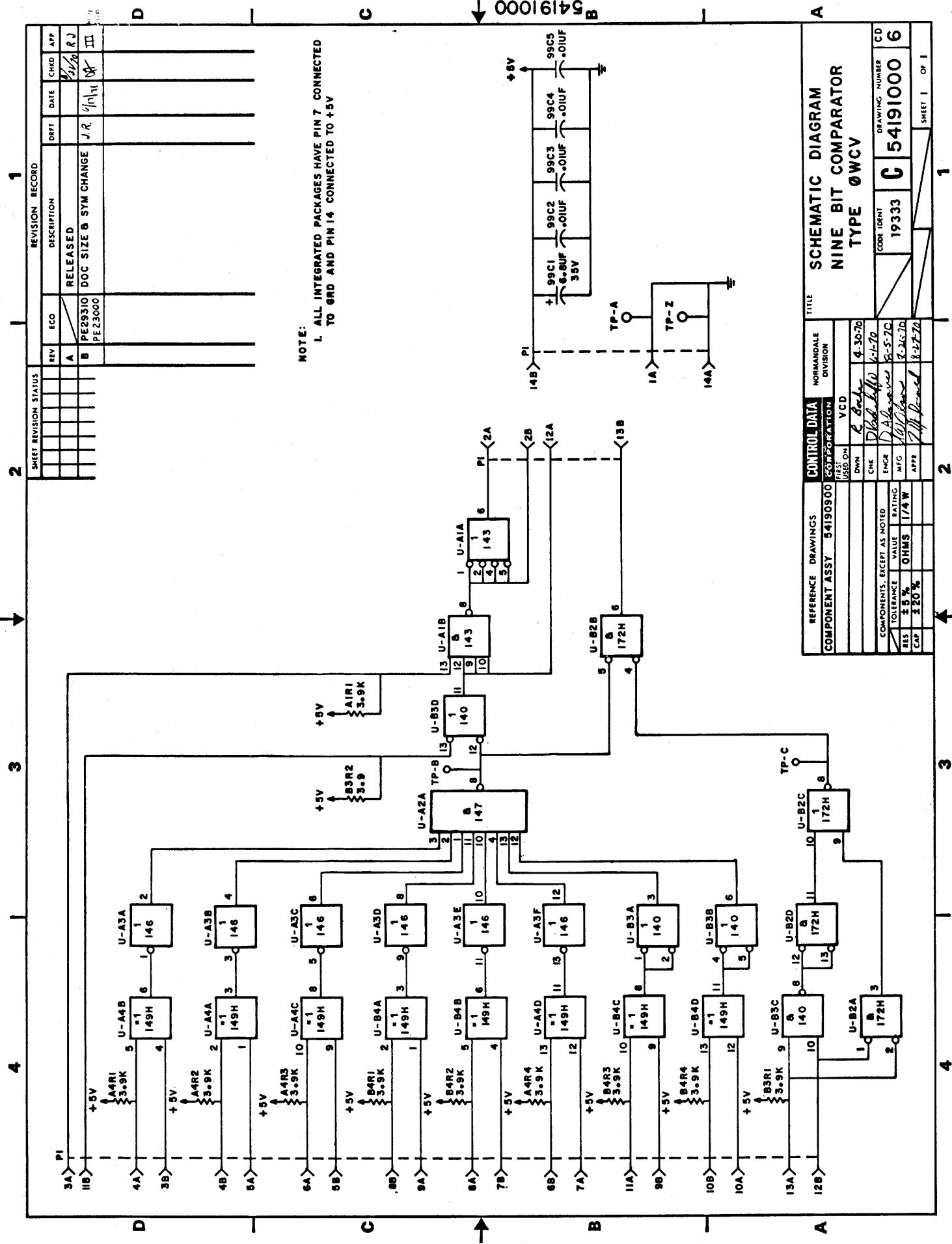




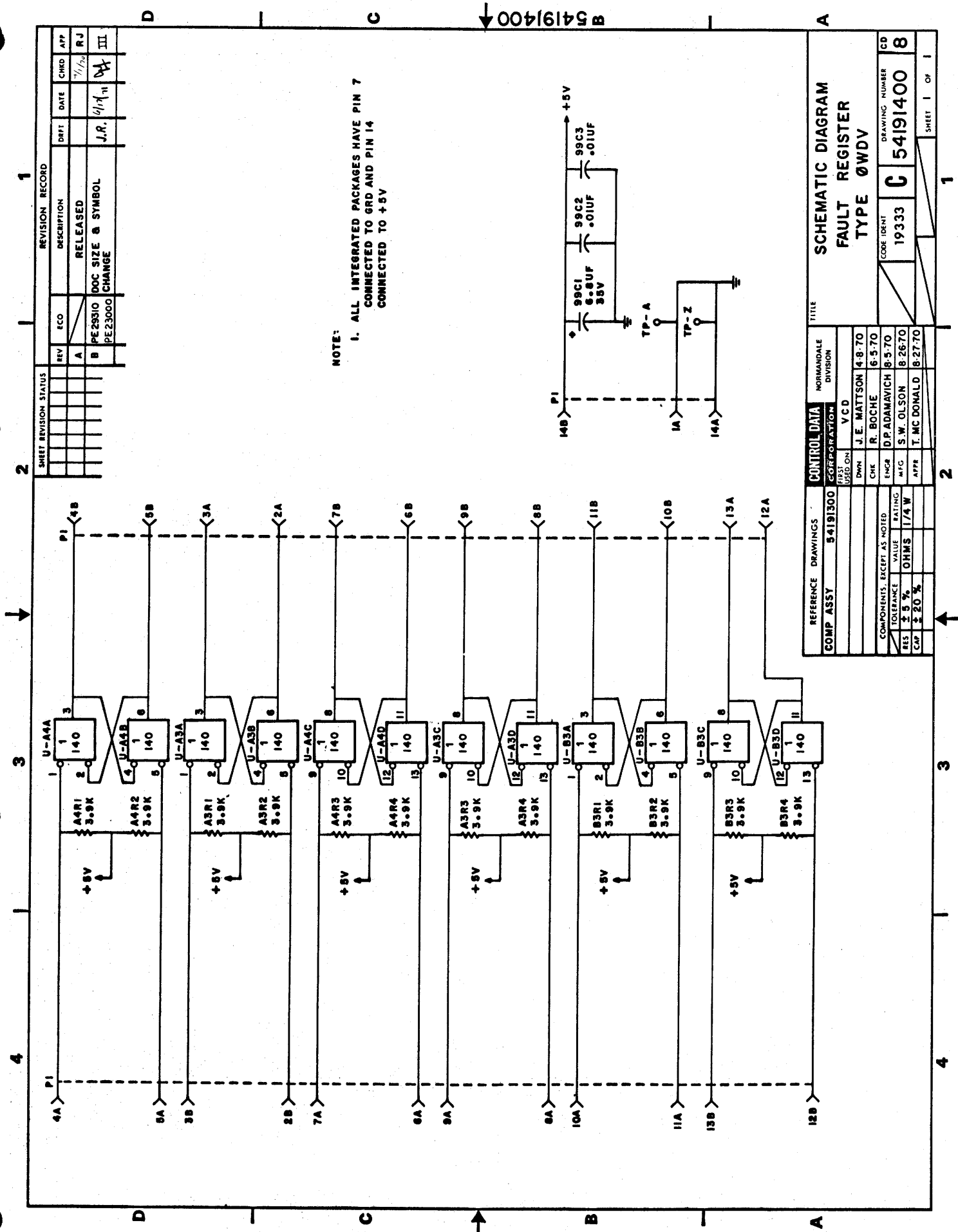


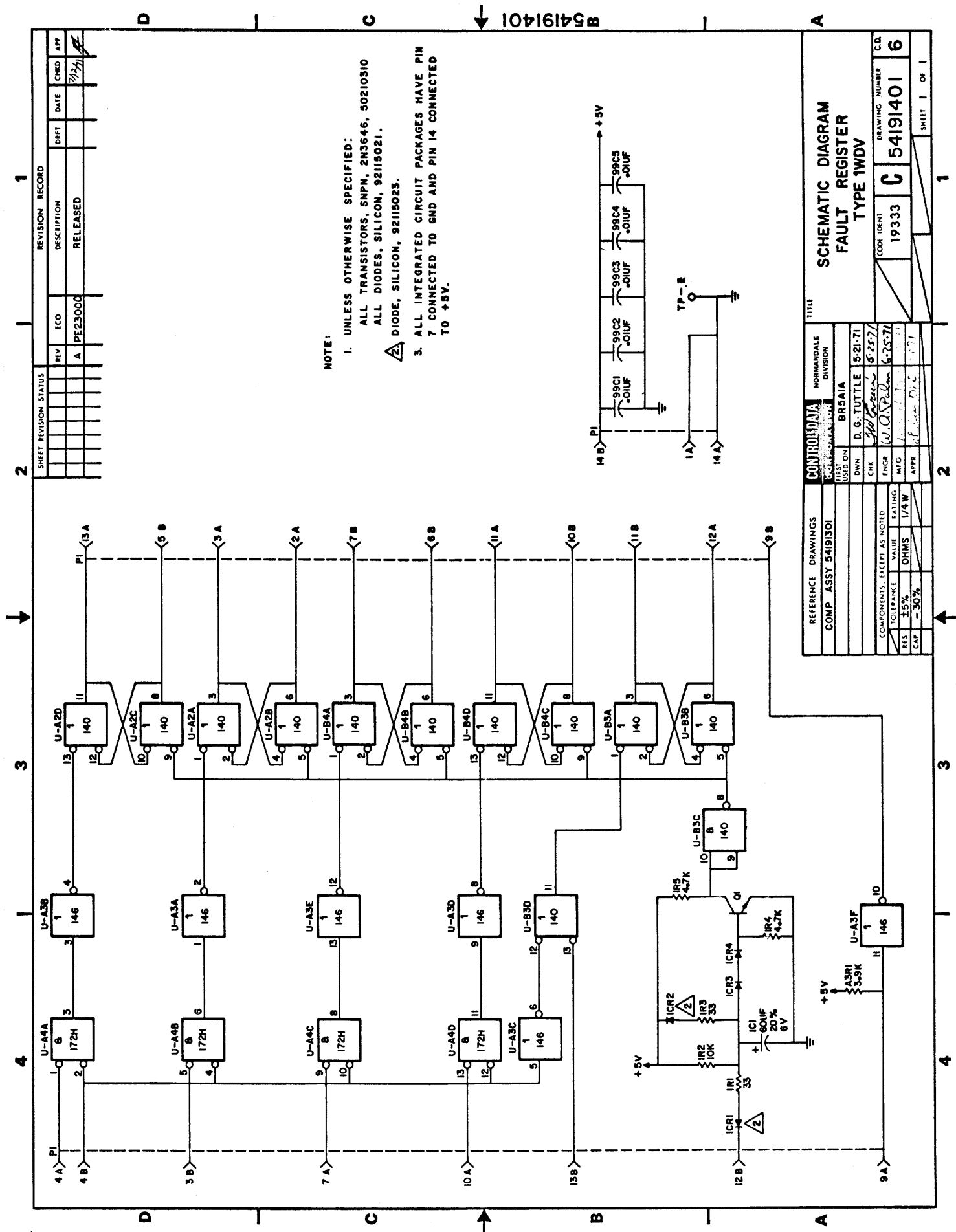
54189400

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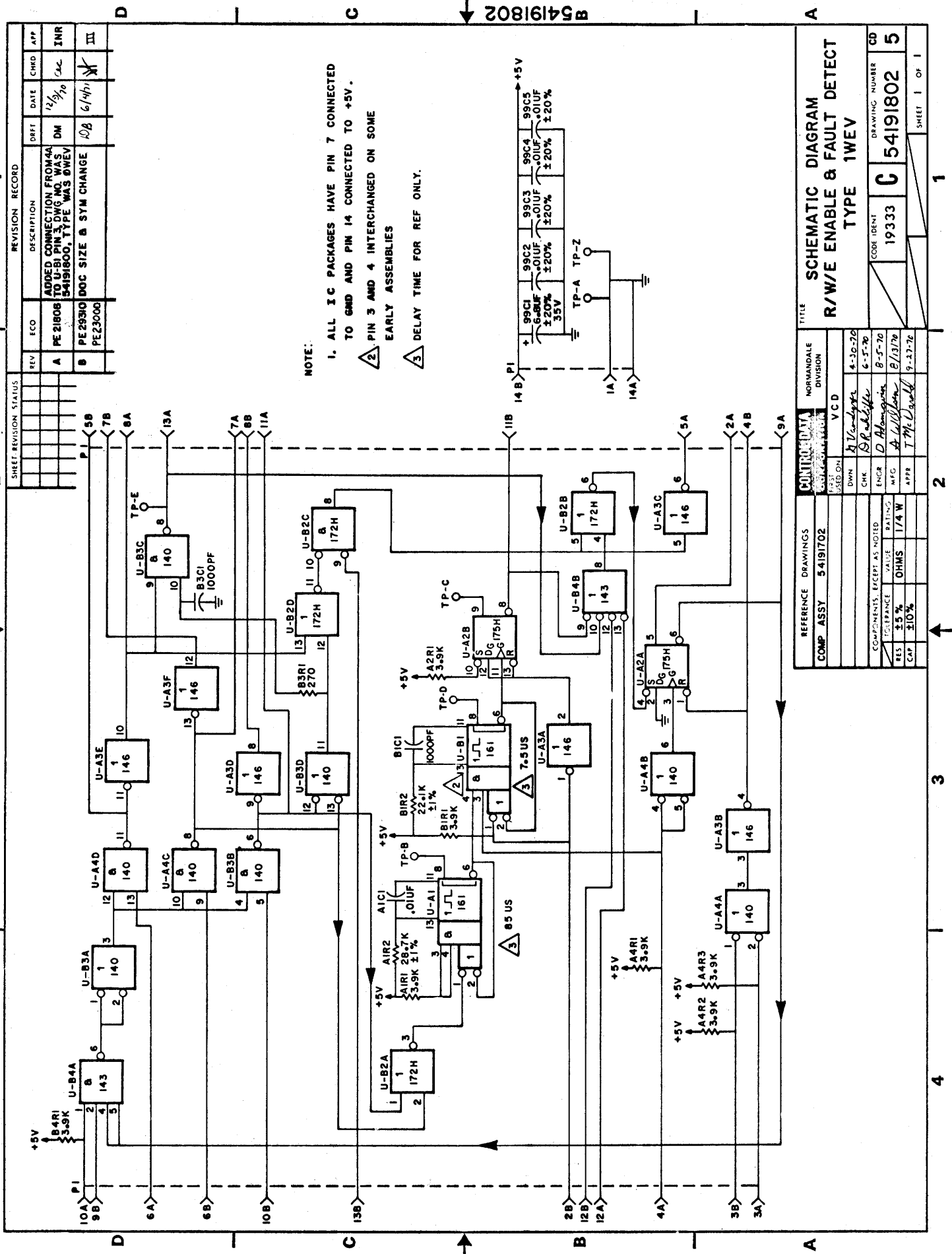


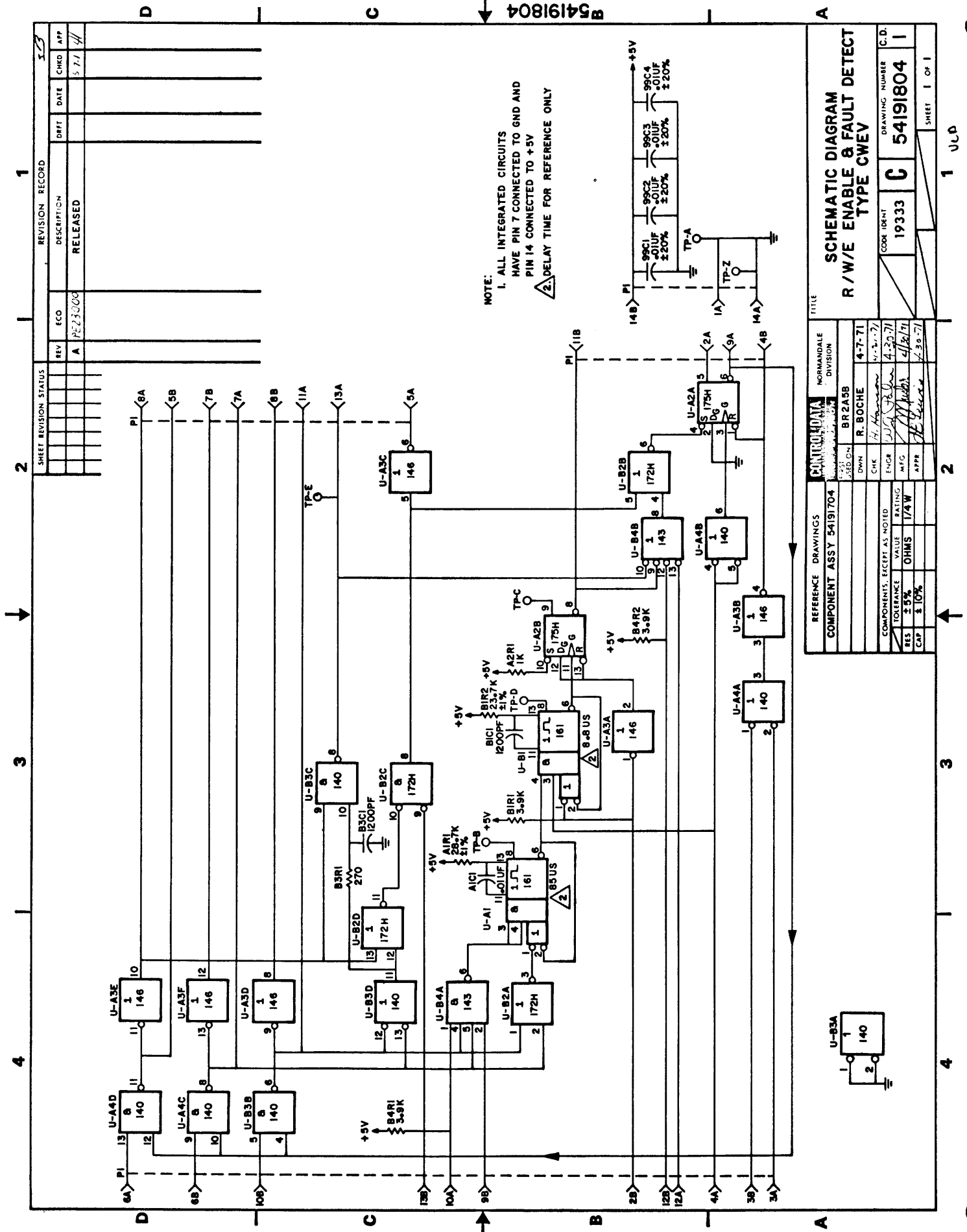
REFERENCE DRAWINGS		CONTROL DATA		NORMANDALE DIVISION		TITLE	
COMPONENT ASSY 54190900		CORPORATION		VCD		SCHEMATIC DIAGRAM	
FIRST USED ON		CHK		DWN		NINE BIT COMPARATOR	
COMPONENTS, EXCEPT AS NOTED		ENGR		MFG		TYPE 0WCV	
TOLERANCE		VALUE		BALING		CODE IDENT	
RES ±5%		OHMS 1/AW		APPR		19333	
CAP 320%						DRAWING NUMBER	
						C 54191000	
						CD	
						6	
						SHEET 1 OF 1	

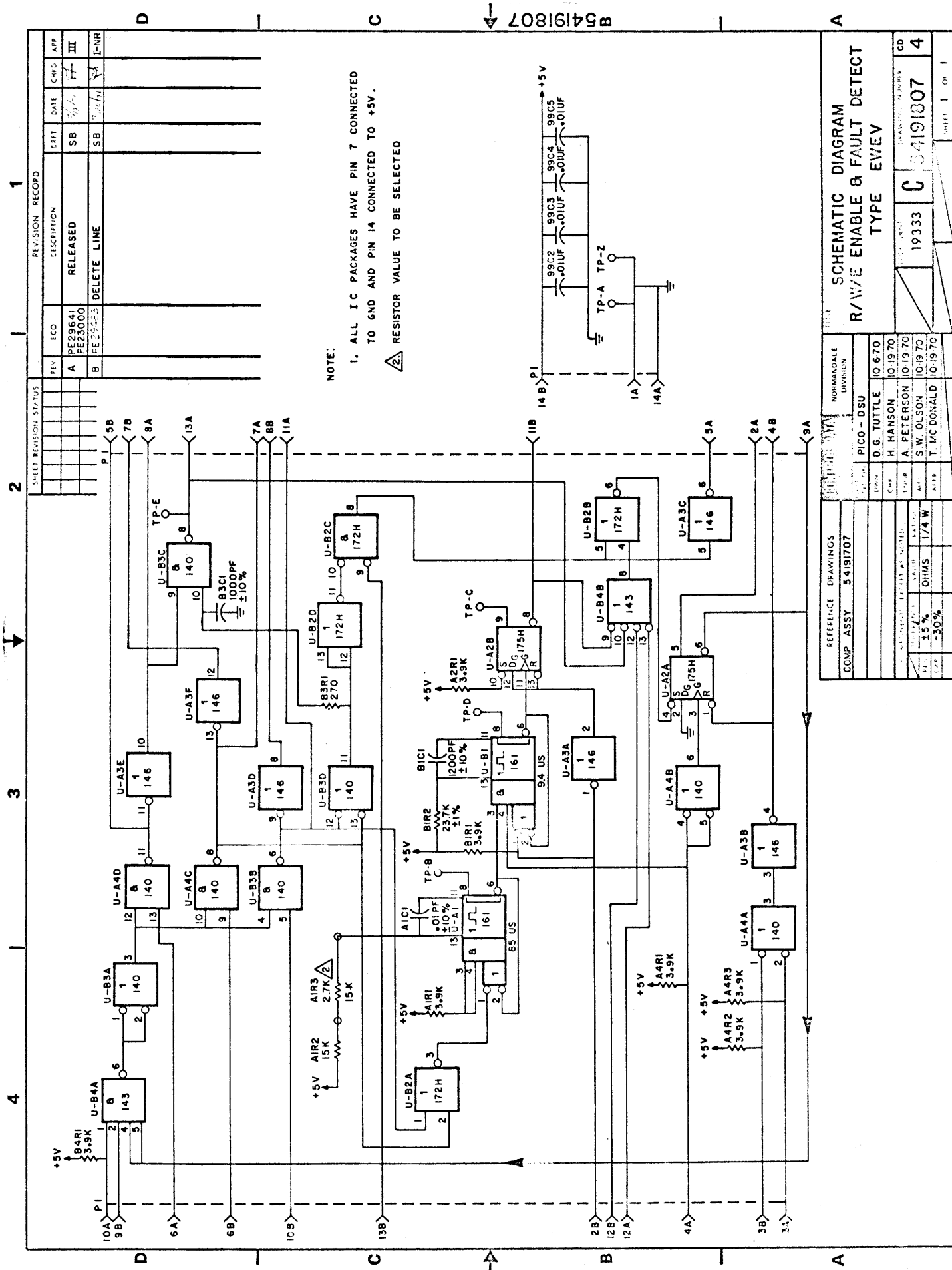




B54191401

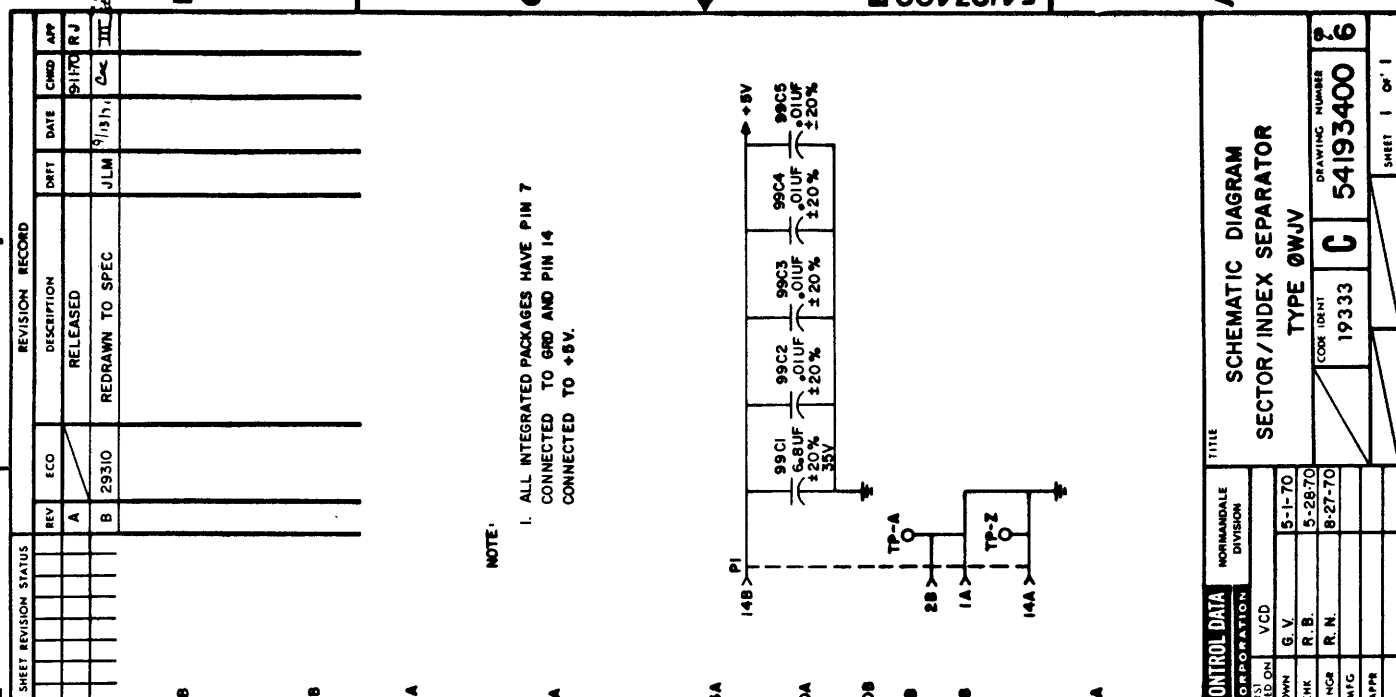


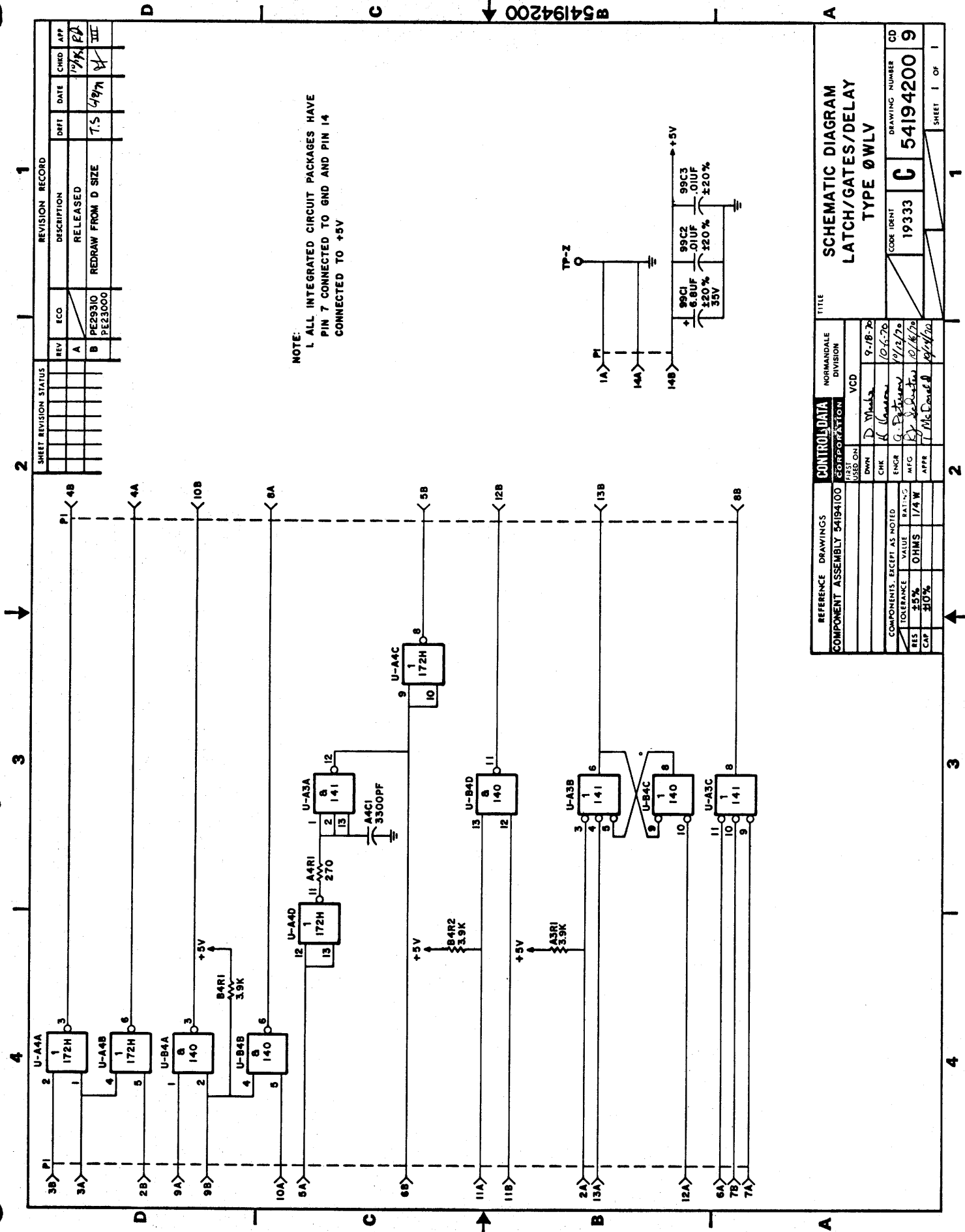




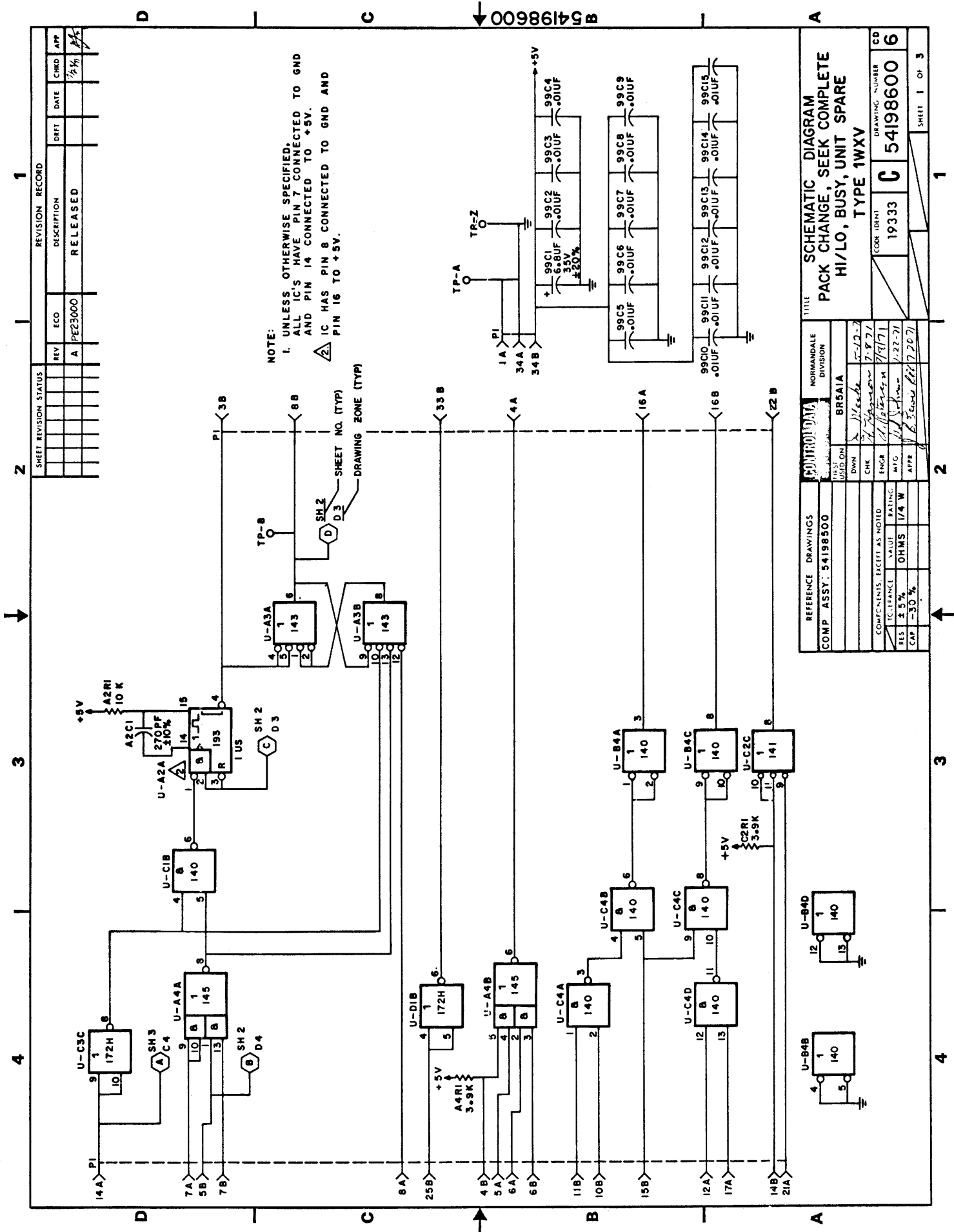
B 54191807

REFERENCE DRAWINGS		TITLE	
COMPONENT ASSY 54192500		SCHEMATIC DIAGRAM UNIT RESERVE TYPE ØWGV	
NORMANDALE DIVISION		DRAWING NUMBER	
VCD		CD	
FIRST USED ON		19333	
G. VANDEGRIFT		C	
D. RADCLIFFE		54192600	
D.P. ADAMAVICH		2	
S.W. OLSON		1	
T. McDONALD		OF 1	
CHK		9-27-70	
ENGR		5-27-70	
MFG		8-21-70	
APPR		9-3-70	
APPR		9-27-70	
COMPONENTS, EXCEPT AS NOTED			
TOLERANCE		VALUE	
RES ± 5%		OHMS 1/4W	
CAP ± 20%			





B54194200



REV	ECO	DESCRIPTION	DATE	CHKD	APP
A	PE23000	RELEASED			

SHEET	REVISION	STATUS
1	1	

REV	ECO	DESCRIPTION	DATE	CHKD	APP
A	PE23000	RELEASED			

SHEET	REVISION	STATUS
1	1	

REV	ECO	DESCRIPTION	DATE	CHKD	APP
A	PE23000	RELEASED			

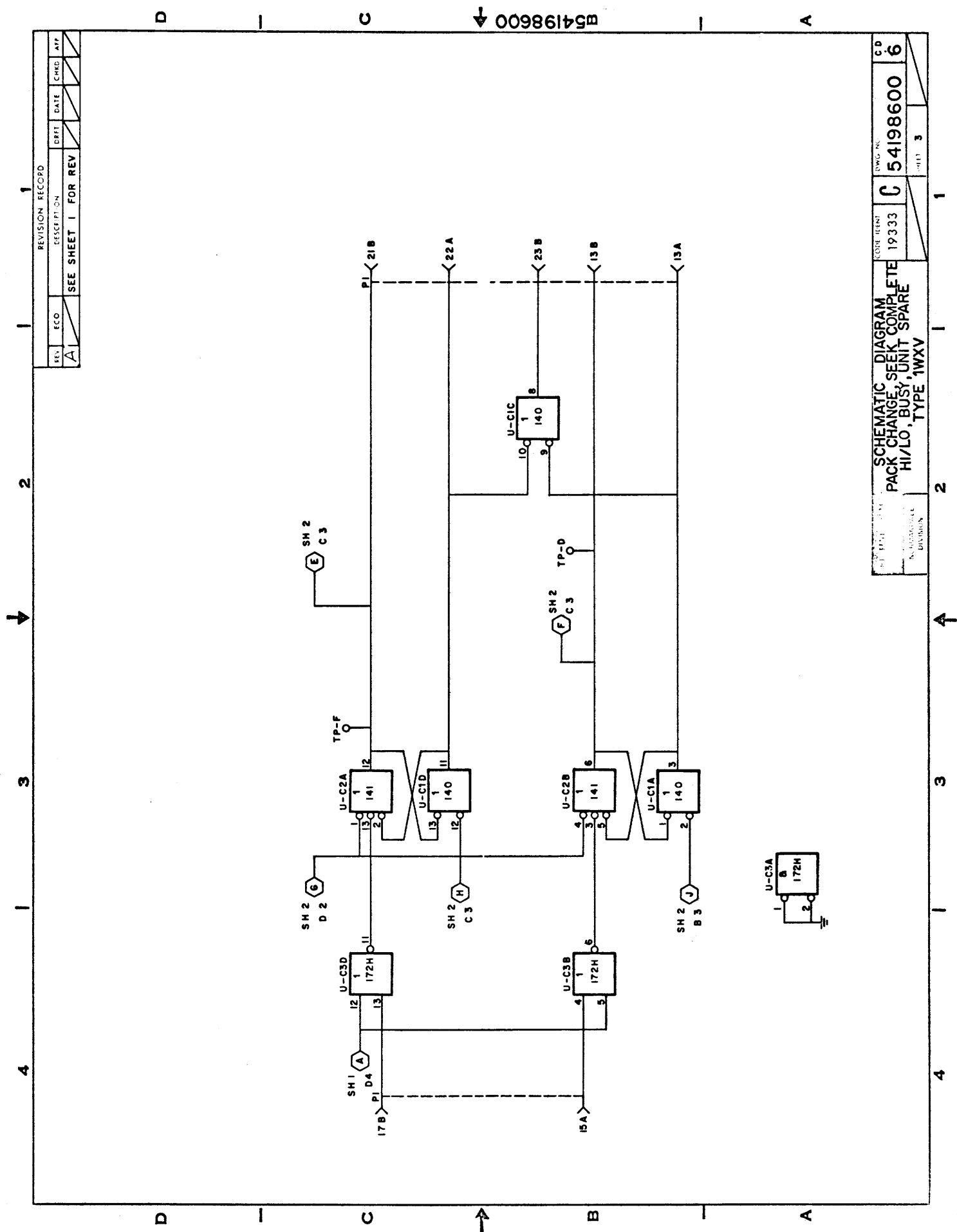
SHEET	REVISION	STATUS
1	1	

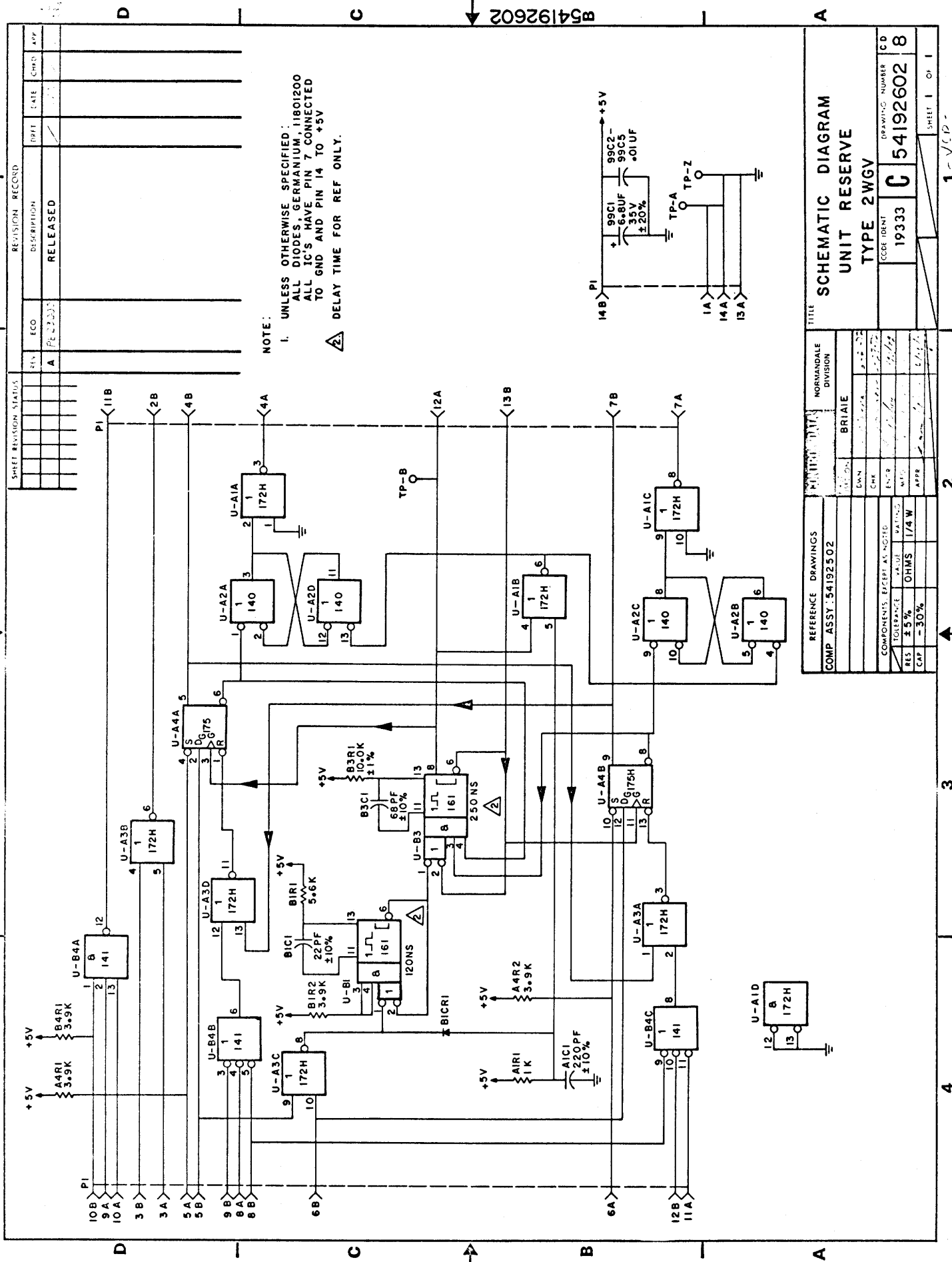
REV	ECO	DESCRIPTION	DATE	CHKD	APP
A	PE23000	RELEASED			

SHEET	REVISION	STATUS
1	1	

REV	ECO	DESCRIPTION	DATE	CHKD	APP
A	PE23000	RELEASED			





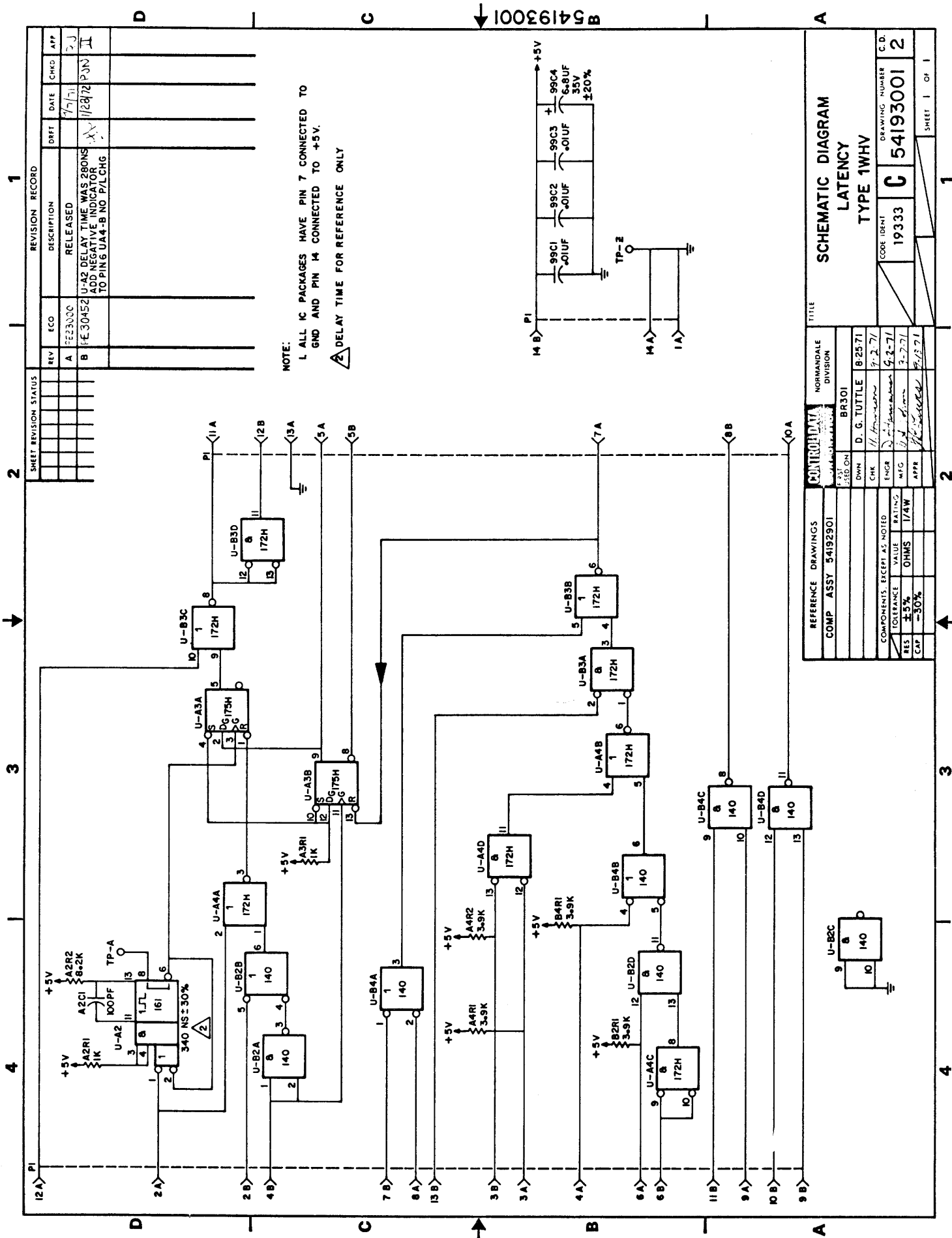


SHEET REVISION STATUS		REVISION RECORD	
REV	ECO	DESCRIPTION	DATE
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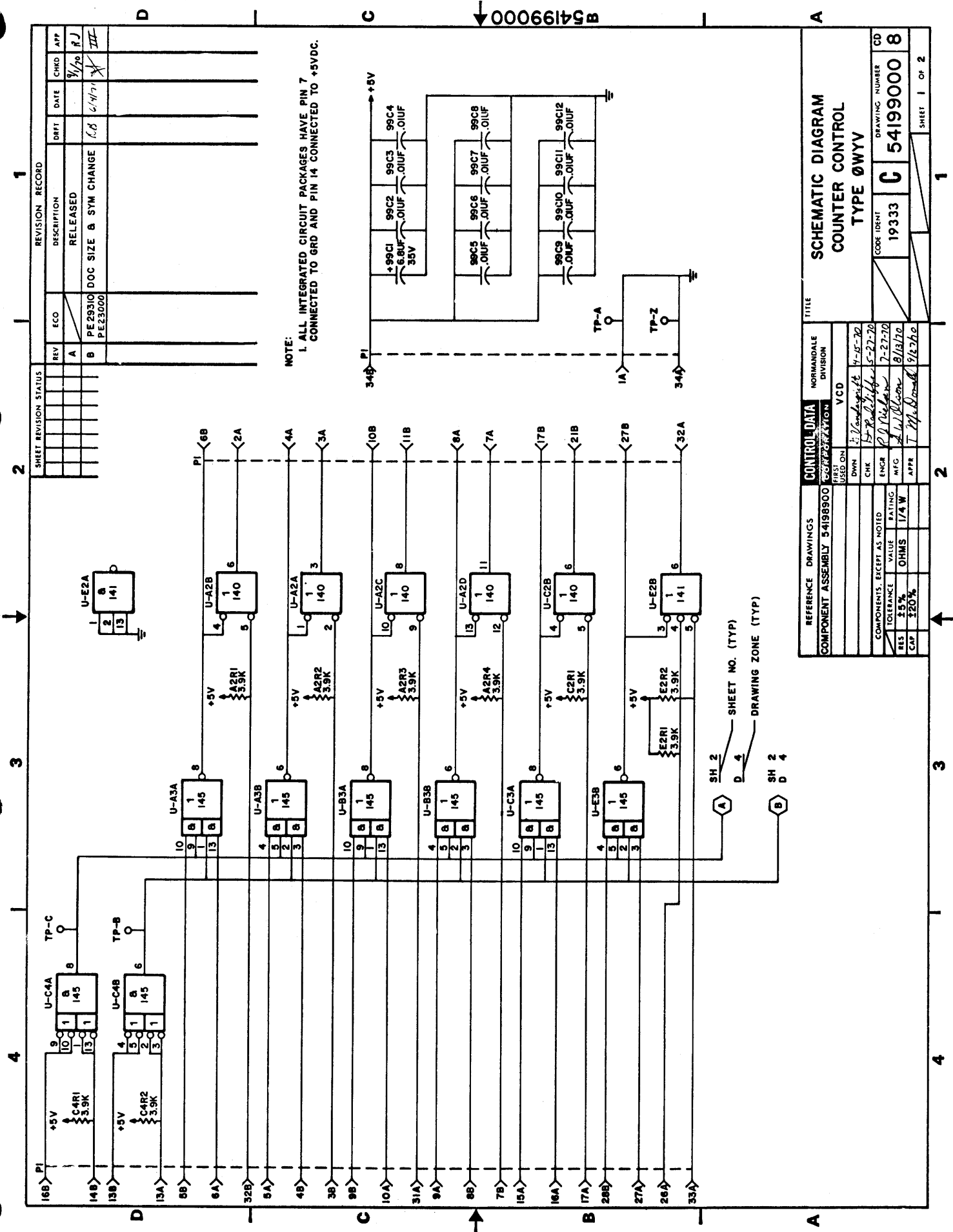
REFERENCE DRAWINGS		NORMANDALE DIVISION	
COMP ASSY	54192502	BR/1A	
COMPONENTS, EXCEPT AS NOTED			
TOLERANCE	±5%	OHMS	1/4 W
RES	±5%	OHMS	1/4 W
CAP	±30%		

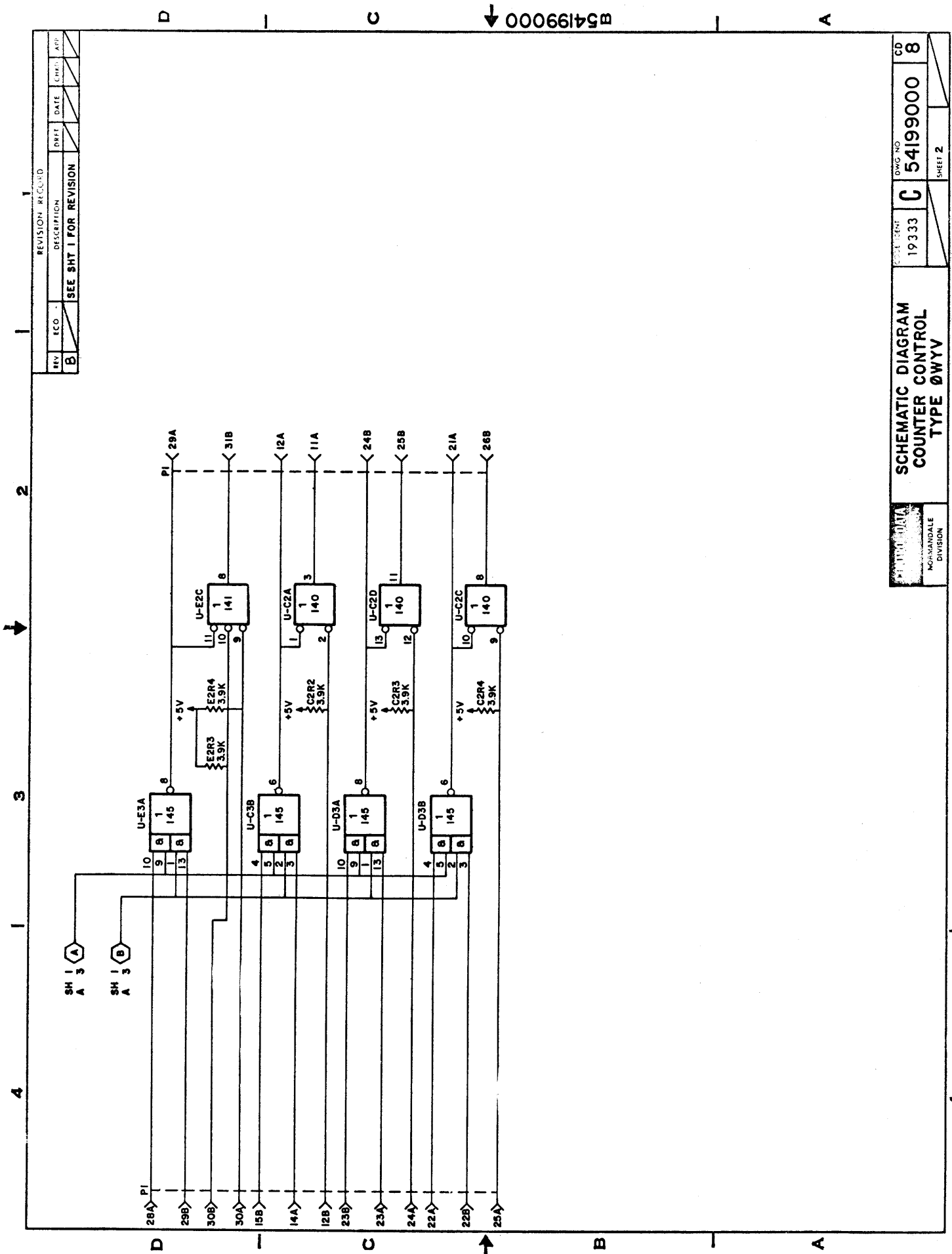
TITLE		DRAWING NUMBER	
SCHEMATIC DIAGRAM		54192602	
UNIT RESERVE		19333	
TYPE 2WGV		C	
SHEET 1 OF 1		1-100	

B54192602

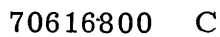


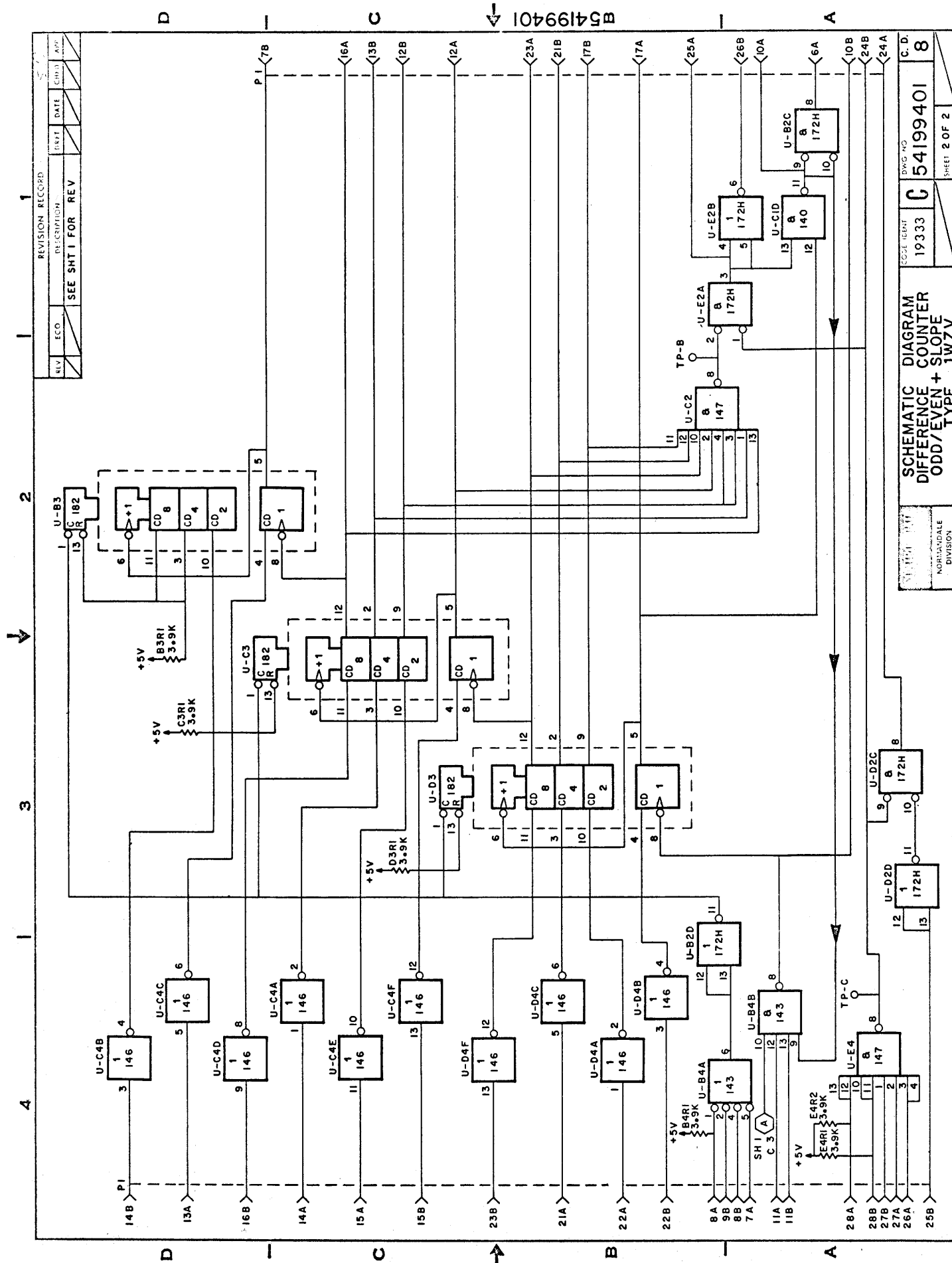
B 54193001





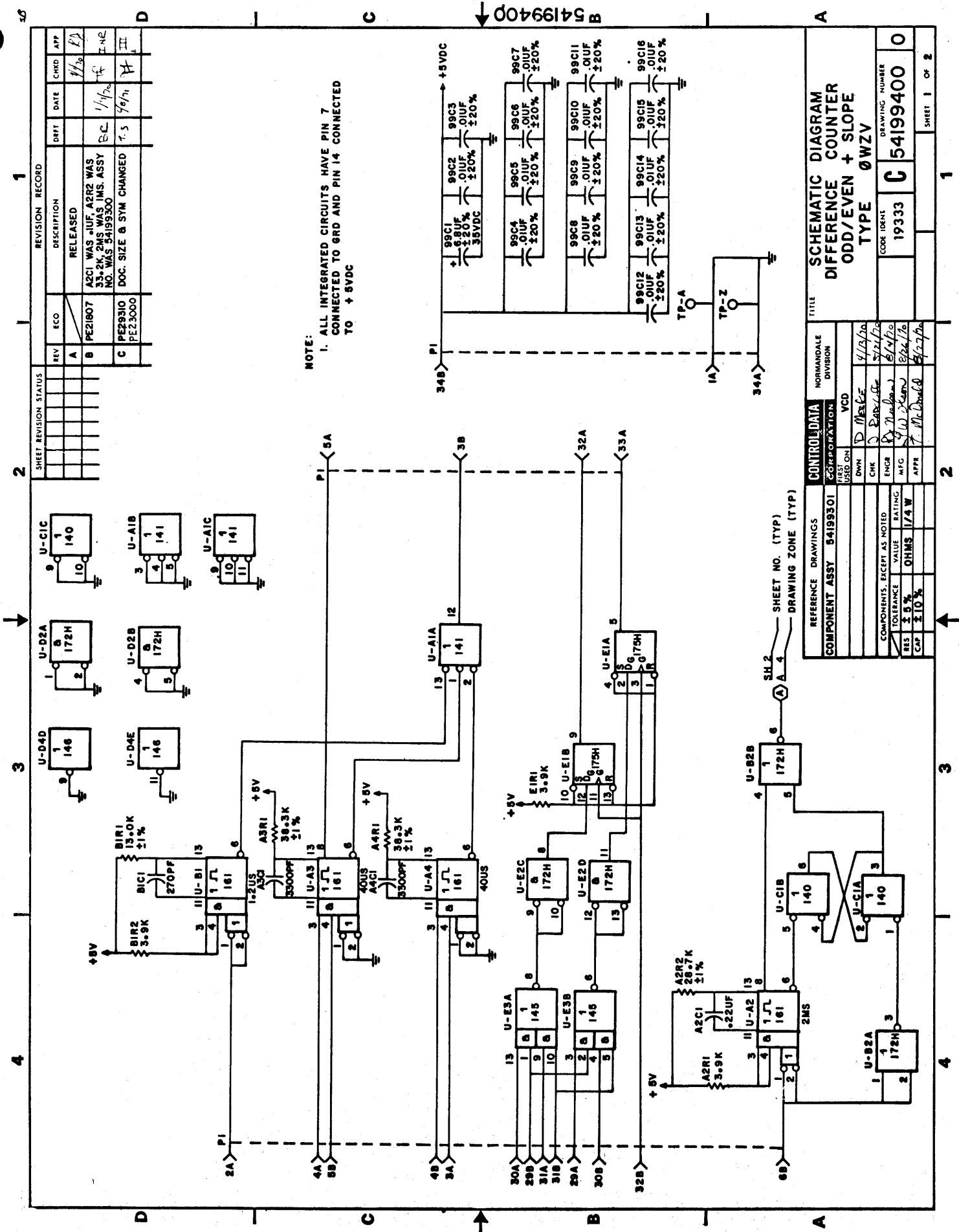
B54199000 ↓





SCHEMATIC DIAGRAM		C 54199401		C.D. 8	
DIFFERENCE COUNTER		19333		DWG. NO.	
ODD/EVEN + SLOPE		TYPE 1WZV		SHEET 2 OF 2	
NATIONAL		DIVISION			

REVISION RECORD					
REV	ECO	DESCRIPTION	DATE	CHKD	APP
1		SEE SMT 1 FOR REV			



PART 3

HEAD AND DISK PACK
REPLACEMENT CRITERIA



HEAD AND DISK PACK REPLACEMENT CRITERIA

HEAD REPLACEMENT CRITERIA

Heads of the DSU have been designed so that they should not need replacement if given proper preventive maintenance and care. If a head requires replacement refer to the Preface of this manual for the publication containing the Maintenance section. Refer to that section for Head/Arm Replacement procedure. A head is defective and needs replacing if any of the following conditions exist:

1. Consistent oxide buildup on head indicating repeated head/disk impact.
2. Appreciable oxide buildup located primarily on the edge of the ferrite insert, indicating a warped head.
3. Oxide or wear over 1/2 of the head face surface.
4. A head which is scratched over 1/2 of the head face surface.
5. Concentric scratches on disk surface. Inspect the head for imbedded particles.
6. Audible ping indicating that the head is hitting the disk surface.

DISK PACK REPLACEMENT CRITERIA

The disk pack is designed to last the lifetime of the equipment. Replacement of the disk pack is required only if excessive runout (see Disk Pack Runout Check) is encountered or physical damage to the pack results in the loss of recording ability.

A disk pack is defective and needs replacement if any of the following conditions exist:

1. Damage to the disk pack resulting in a bent or broken disk. If a disk is bent perform Disk Pack Runout Check procedure.
2. Gouged or scored disk surface causing the loss of stored data.
3. Imbedded particles in a disk surface that cannot be removed by cleaning and are causing damage to the heads.

Disk Pack Runout Check

This procedure determines whether a bent disk pack may remain in use. If the disk pack fails to meet the requirements of the procedure, it should be returned to the manufacturer for reconditioning.

1. Open cabinet top cover.
2. Install the disk pack to be checked on a DSU spindle.
3. Grasp the pack cleaning brushes, override the shaft detent mechanism, and rotate the brushes into the disk pack.
4. Place the disk pack runout gage (P/N 84357600) base on the DSU deck base plate (Figure 7-70) adjacent to disk cleaner cutout in shroud.
5. Turn the bezel of the dial indicator to indicate zero. Orient the dial indicator so that the plastic tip is not only contacting a disk surface but is deflected for an indication of approximately 0.020 inch. Tighten dial indicator in this position. Turn the bezel to set the dial indicator to zero.

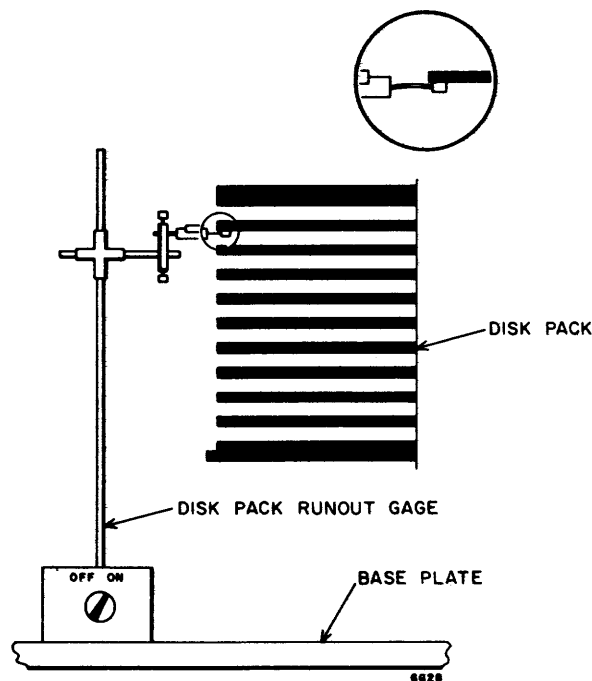


Figure 7-70. Disk Pack Runout Check

NOTE

A mirror is required to observe dial indicator when some disk surfaces are checked.

6. Manually and slowly rotate the disk pack one full revolution while carefully observing the dial indicator. The sum of the deviations (to either side of zero) should not exceed 0.012 inch.
7. If a total deflection of 0.012 inch is encountered in step 6, recheck the indication. The total deflection must occur in a disk circumference of 4 inches or more.
8. Repeat steps 5 through 7 for the 19 remaining disk surfaces.
9. Rotate the pack cleaning brushes clear of the disk surfaces.
10. Remove the disk pack and the disk pack runout gage.

ACCESS TESTER CARD

The access tester card (p/n 54116100) is a special tool used optionally with some DSU's to perform off line maintenance procedures of Section 6. Figure 7-71 is the logic drawing for the card and is provided as an aid in using the tester. Erroneous and/or misleading positioning of the actuator will occur if the tester is not used as specified in the Operation paragraph.

OPERATION

The access tester card allows DSU positioning to be performed in one of two basic modes: repeat (continuous, alternate forward and reverse seeks between a specified pair of tracks) and incremental (sequential seeks of a specified length to the forward limit, returning to zero, and repeating). The desired mode is selected in accordance with the setting of the IN/RP (incremental/repeat) switch, S4. Operation in either mode is controlled by the R/S (run/stop) switch, S3, and the ST (start) switch, S1. A single step modification of the two basic modes may also be performed.

Repeat Mode (Figure 7-72)

To exercise a DSU in the repeat mode, perform following procedure:

1. Set DSU logic chassis maintenance panel ON LINE/OFF LINE switch to OFF LINE and set DC switch to OFF.
2. Install access tester card in DSU logic chassis location C30.
3. Set DC switch to ON.
4. Install disk pack on DSU spindle.
5. Start spindle motor and allow brush cycle to end.
6. Press tester RT (return to zero) switch, S2. DSU should load heads and return to track 0.
7. Set tester IN/RP switch to RP position (repeat).
8. Set tester R/S switch to R position (run).
9. Set tester FWD switches to binary equivalent of the higher valid track desired during the seek. (Example: To select track 100, set FWD switches 64, 32, and 4 to 1. Set other switches to 0).
10. Set tester REV switches to binary equivalent of the lower valid track desired during the seek. (Example: To select track 10, set REV switches 8 and 2 to 1. Set other switches to 0).

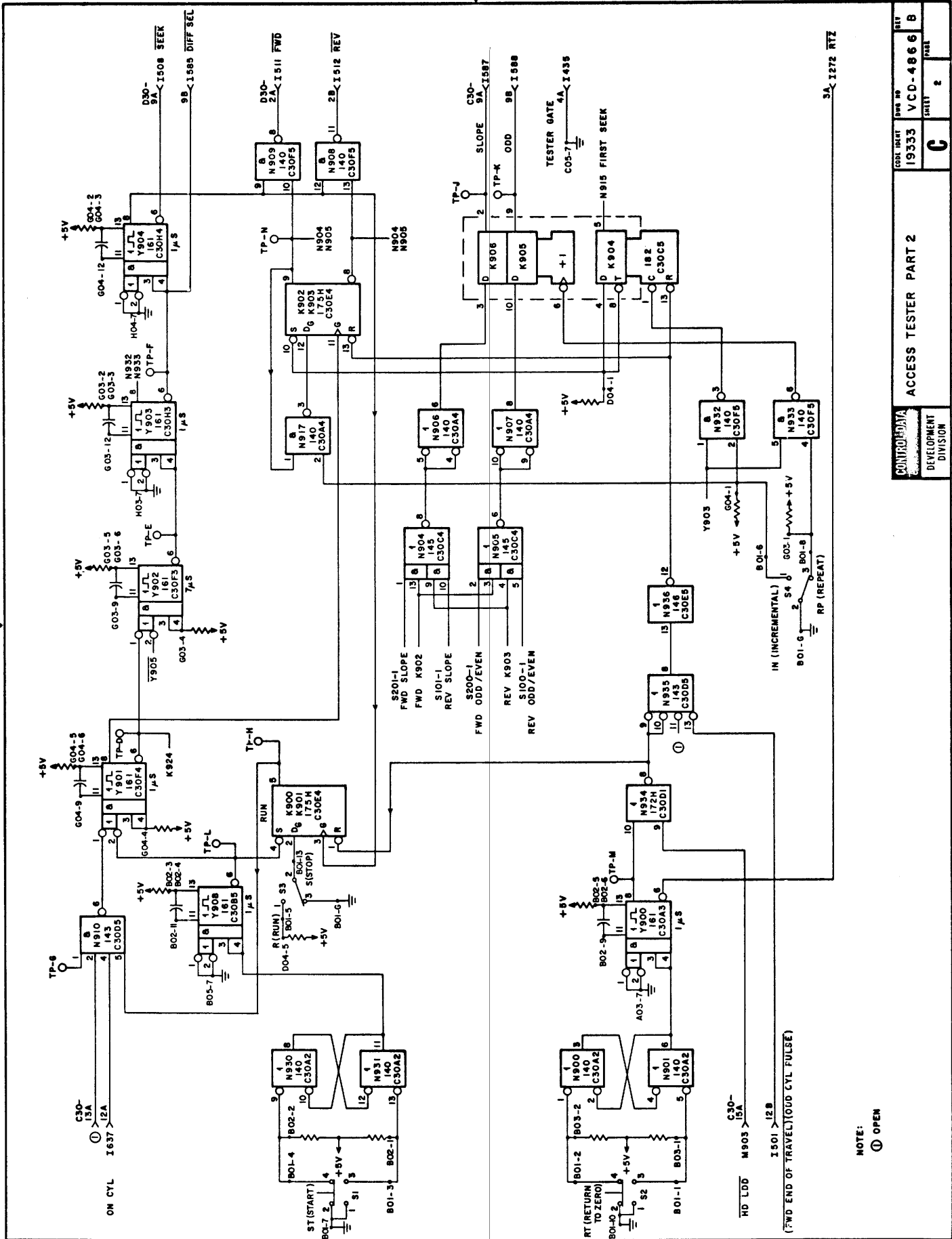
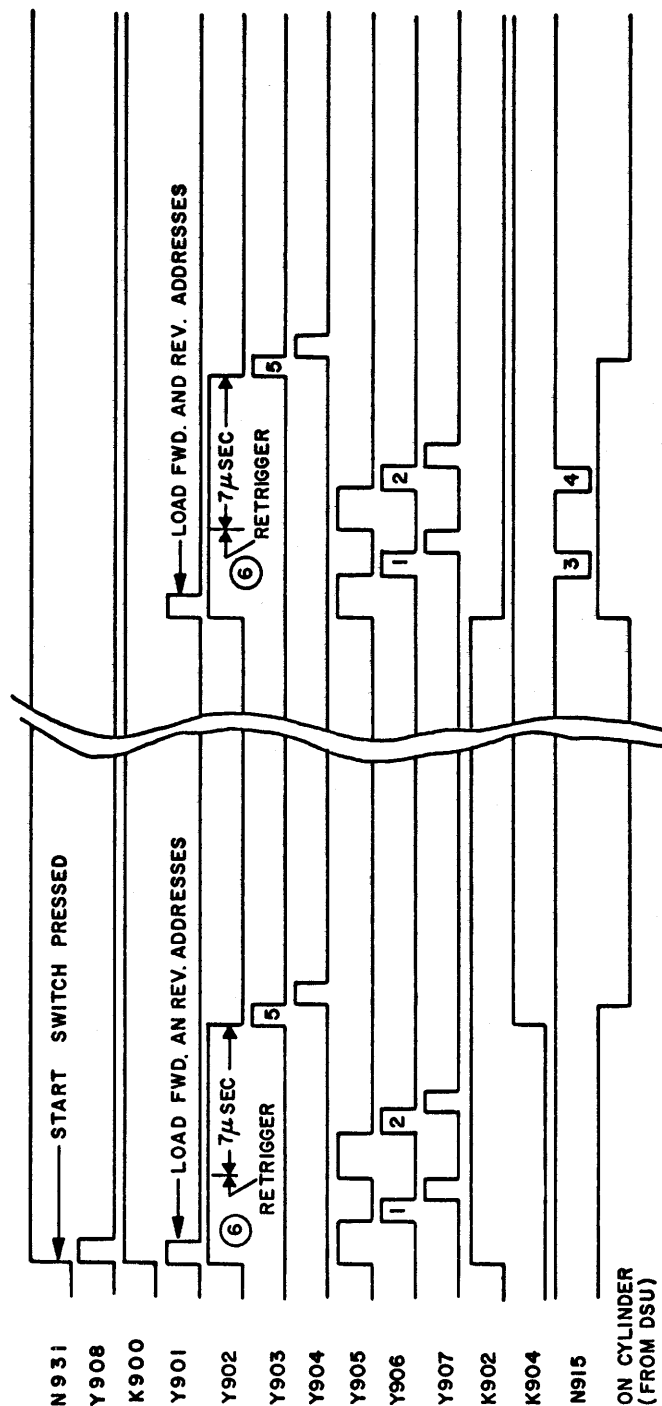


Figure 7-71. Access Tester Card Logic - (Sheet 2 of 2)

REPEAT SEEK (CYLINDER 4 TO CYLINDER 2)



1. INCREMENT REVERSE COUNTER CONTENT 11111101 → 11111110
2. " " " 11111110 → 11111111
3. INCREMENT FORWARD " " 11111101 → 11111100
4. " " " 11111100 → 11111101
5. DELIVER DIFFERENCE FROM FORWARD COUNTER TO DSU DIFFERENCE COUNTER.
- ⑥ Y902 RETRIGGERED BY Y905 EVERY 4μSEC UNTIL REVERSE COUNTER IS INCREMENTED TO ALL ONES.

6T175

Figure 7-72. Repeat Mode Timing

11. Press tester ST switch.
12. The DSU should now seek forward to the track specified by the FWD switches, generate an On Cylinder signal, seek in reverse to the track specified by the REV switches, and generate an On Cylinder signal.
13. The activities of step 12 will continue until either the tester RT switch is pressed or the R/S switch is set to the S position (stop).
14. Set DSU DC switch to OFF before removing tester card from logic chassis.

Incremental Mode

To exercise a DSU in the incremental mode, perform the following procedure:

1. Set DSU logic chassis maintenance panel ON LINE/OFF LINE switch to OFF LINE and set DC switch to OFF.
2. Install access tester card in DSU logic chassis location C30.
3. Set DC switch to ON.
4. Install disk pack on DSU spindle.
5. Start spindle motor and allow brush cycle to end.
6. Press tester RT (return to zero) switch, S2. DSU should load heads and return to track 0.

NOTE

This procedure is written for a one-track incremental seek. Other, but not all, increments may be selected. Valid selected increments are restricted to those where the FWD switch 1 is set to 1 and the FWD switch 2 is set to 0. Remaining FWD switches (4 through 256) may be set as desired. Settings other than the aforementioned, will result in unpredictable seek activity.

7. Set tester FWD switch 1 to 1.
8. Set all other FWD and REV switches to 0.
9. Set tester IN/RP switch to IN position (incremental).
10. Set tester R/S switch to R position (run).
11. Press tester ST switch.
12. The DSU should now seek forward, one track at a time, until the forward limit is reached, at which time the logic chassis maintenance panel FAULT indicator lights (indicates seek error). To recover from the seek error, the DSU will automatically

return to track 0 and again seek forward, one track at a time.

13. The activities of step 12 will continue until either the tester RT switch is pressed or the R/S switch is set to the S position (stop).
14. Set DSU DC switch to OFF before removing tester card from logic chassis.

Single Step

To exercise a DSU in either a repeat single step mode or an incremental single step mode, perform following procedure:

1. Perform either the procedure for repeat mode operation or the procedure for incremental mode operation, except when the applicable procedure directs positioning of R/S switch, set it to S (instead of R).
2. Now, when the tester ST switch is pressed (step 12 of both procedures), the DSU will perform one seek operation and stop.
3. Press tester ST switch each time a seek operation is desired.

READ/WRITE TESTER CARD

The R/W tester card (p/n 54113701) is a special tool used optionally with some DSU's to perform off line maintenance procedures of Section 6. Figure 7-73 is the logic drawing for the card and is provided as an aid in using the tester.

OPERATION

The R/W tester card allows checkout and diagnosis of the read/write circuits in a DSU.

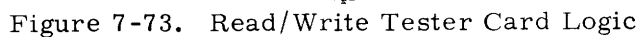
Write Operation (Figure 7-74)

To write on a DSU disk pack, perform following procedure:

1. Set DSU logic chassis maintenance panel ON LINE/OFF LINE switch to OFF LINE and set DC switch to OFF.
2. Install R/W tester card in DSU logic chassis location C21.
3. Set DC switch to ON.

CAUTION

A CE disk pack contains specially recorded tracks of data. Extreme care must be taken so that this data is not modified. Read or write circuit diagnosis or testing should be done using an unrecorded disk pack or one containing expendable data (scratch pack).



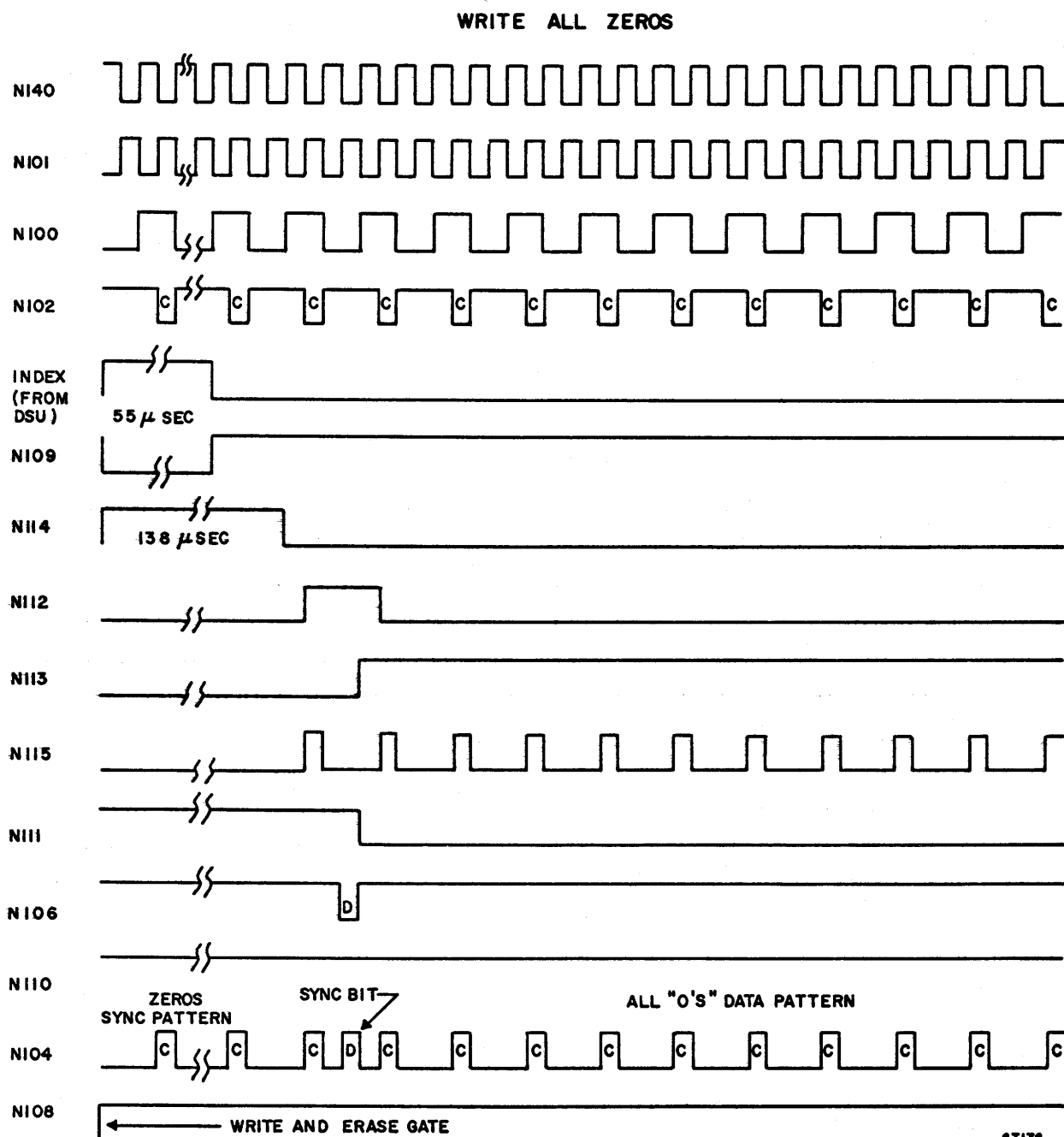


Figure 7-74. Write Operation Timing - All Zeros

4. Install a scratch pack on DSU spindle.
5. Start spindle motor and allow brush cycle to end.
6. Select desired data pattern to be written by setting tester switches as follows:

Desired pattern	1-0 switch (S1)	ONE switch (S2)
All "1's"	OFF	OFF
All "1's"	ON	OFF
All "0's"	ON	ON
Alternate "1's" and "0's"	OFF	ON

7. Set tester W (write), E (erase), and C-S (control select) switches to ON.
8. Set tester R (read) switch to OFF.
9. Position DSU heads to desired track. (Positioning may be manually, using access tester card, or central processor).
10. Set tester binary switches (1 through 16) representing binary equivalent of desired head to the right. (Example: To select head 11, set switches 8, 2, and 1 to the right. Set switches 4 and 16 to the left).
11. Set tester EN (enable) switch to ON.
12. When the leading edge of Index (Figure 7-74) is sensed, a 138 usec sync pattern of all "0's" is written. This is followed by a single data "1" sync bit and finally the pattern selected by switches S1 and S2 is written until the next leading edge of Index.

NOTE

The positions of the binary switches used to select a head may be changed during a write operation without affecting a read recovery.

13. The activity of step 12 will repeat until one of the following occurs:
 - If W, E, or C-S switch is set to OFF, the write operation will stop immediately
 - If EN switch is set to OFF or a DSU not On Cylinder occurs, the write operation will stop with the next Index pulse.
14. Refer to Read Operation paragraph to recover written pattern.

Read Operation

The tester read recovery circuit is a simple discriminator designed to recover a pattern written during the above described Write Operation. The tester incorporates no checking logic, and pattern verification can be made only by monitoring the D (data) and C (clock) test jacks with an oscilloscope. Use the tester S (sync) test jack to trigger the oscilloscope.

To read from a DSU disk pack, perform the following procedure:

NOTE

Following procedure assumes that tester was installed in DSU logic chassis to write a pattern, and now a read recovery of the pattern is to be performed.

1. Set tester W and E switches to OFF.
2. Set R and C-S switches to ON.
3. Set tester binary switches representing binary equivalent of desired head to the right. (Example: To select head 15, set switches 8, 4, 2, and 1 to the right. Set switch 16 to the left).
4. Set tester EN switch to ON.
5. When the leading edge of Index is sensed, tester generates Read Gate. Tester discriminator circuit then uses the 138-usec "0's" pattern to get in sync. When single-shot N116 times out (noise blanking), the recovered data "1" sync bit sets the Sync FF, N121. Then follows recovered data and clock pulses which the tester separates for monitoring (inverted) at the D and C test jacks.
6. The activity of step 5 will continue until the R, C-S, or EN switch is set to OFF.
7. Set DSU DC switch to OFF before removing tester card from logic chassis.



SECTION 8

PARTS DATA

Information for this section is included in Disk Storage Unit Parts Data Manual.

SECTION 9

WIRE LISTS

Information for this section is included in Disk Storage Unit Diagrams, Wire Lists Manual

SECTION 10

EQUATION SUMMARY

(Not Applicable)



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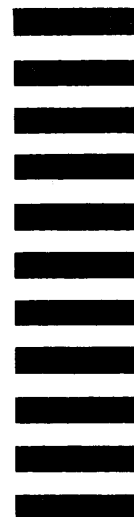
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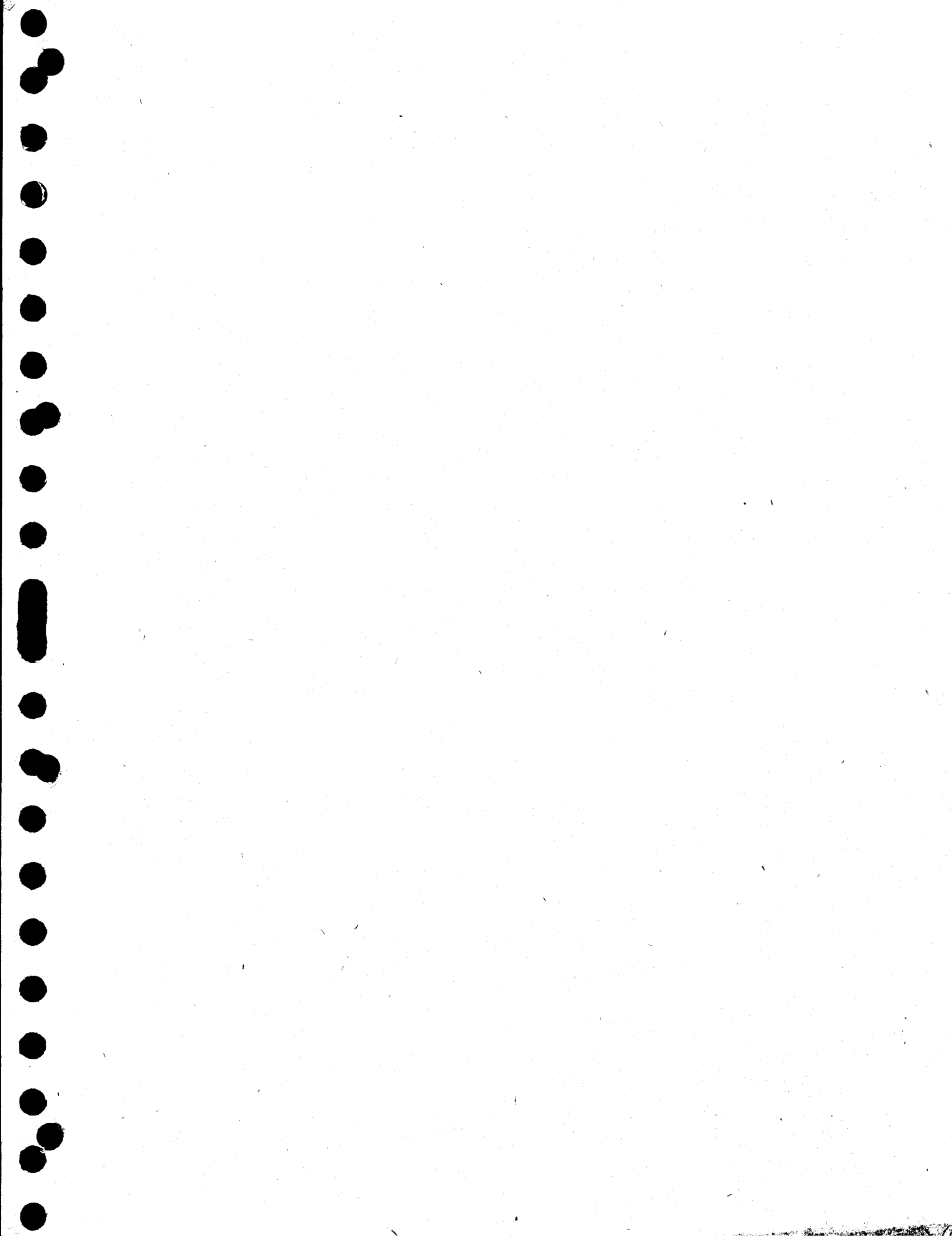
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